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REDUCTION REQUIREMENTS FOR DATA ACQUIRED
BY AN AIRBORNE DATA LOGGER

by

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Summary

Methods to be used for reducing data recorded with an airborne magnetic tape recorder, in both analogue and digital form, are described. Most of the analogue recording uses frequency modulation techniques and the digital recording uses either a special serial format or a parallel format (where only digital data has to be recorded).

Digital computer interface equipment, which has been developed to handle the format of the digitally recorded data, is described in detail. Included is a description of a novel “electronic flywheel” circuit which detects data gaps, used for word and frame synchronization, over a wide range of data rates. Such a circuit could be used in many other applications whenever insertion of missing clock pulses in a pulse train is required.

The recording of time-of-day in digital form allows for correlation of data reduced at different times. Data recorded in analogue form may be readily correlated with data recorded in digital form. Location of any point of interest on the recorded tape is simplified by a preset stop facility which allows the analogue tape machine to be stopped at any preset time of recording.

At the time of writing most of the circuits described for use with the serial type digital recording have been checked (those for use with the parallel system are scheduled for checking later).
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1. INTRODUCTION

Using an airborne data acquisition system which has recently been devised, data will be recorded on an analogue magnetic tape machine using both analogue and digital techniques. Before the system as formulated can be operational, some development is required to realize a fully functional unit designed to meet the very exacting requirements of airborne equipment. The main development area is in relation to recording using digital techniques. This development is currently being undertaken at these laboratories.

Concurrently with the development of the airborne equipment, the ground station data reduction requirements are being considered. In order to assess the airborne data acquisition system and, in particular, to check error rates for the digital system, it is essential that at least part of the ground station reduction equipment be available. It is envisaged that data recorded using digital techniques will eventually be analysed with the aid of a digital computer and data recorded using analogue techniques will be analysed using either analogue data reduction equipment or a digital computer (after suitable conversion of the analogue data to digital form). Because of the unusual aspects of the recording system some special data reduction techniques have had to be investigated.

One of the essential requirements of the data acquisition system is that it produce a recording which allows time correlation between data recorded using analogue and digital techniques to be obtained. The recording of time-of-day on one of the multiplexed digital channels provides a basic identifier which enables data reduced at different times (with different equipment possibly) to be correlated in time. However, since the magnetic tape records may be required to be reproduced at any speed (in octave steps) between 1½ inches per second and 60 inches per second (the range of tape speeds available in both the airborne recorder and the ground station reproducer) it is essential that the reduction equipment be capable of reading time-of-day information at any of these speeds. This requirement is markedly different from that for most digital systems in which the data is read at one specific rate only.

To accommodate the variable data reading rates an "electronic flywheel" circuit has been devised. The "electronic flywheel" forms part of special digital interface equipment which has been developed to enable analysis of the recorded digital data using a digital computer. Because of the wide field of possible application of this circuit and its novelty, it is described in detail.

The overall requirements of the ground station data reduction equipment are analysed in this paper and some circuit developments are described. Greatest emphasis is placed on the description of the ground station digital interface equipment. In general the various sub-sections of the digital interface equipment are described firstly in broad terms, then in somewhat greater detail with derivation of the logic sequences and reference to particular circuit components.

2. TYPES OF DATA REQUIRING REDUCTION

The recording techniques which have been adopted for different types of data have already been outlined. However, some small modifications and extensions have since been incorporated. Details of these modifications and extensions together with a brief résumé of the recording techniques will be given in this section.

Direct recording techniques will be used chiefly for the recording of a composite signal, containing speech and reference frequency information, on a single recording track. The reference frequency recorded is changed when the tape speed is changed and will be used for servo speed control of the reproducing machine. The frequencies used correspond to those specified by IRIG (100 kilohertz at 60 inches per second tape speed and proportionately lower at lower tape speeds).
Frequency modulation (FM) techniques will be used extensively for the recording of data involving large bandwidths. One of the proposed extensions is a time multiplexing capability for data to be recorded using FM techniques. In the system originally proposed each measurement channel required a separate recording track. When two tracks are allocated for digital recording and one for direct recording only four tracks are left for FM recording. Frequently however many more measurements are required over large bandwidths. Such a requirement is particularly likely for vibration recording where triaxial transducer blocks are frequently employed to provide the vibration components in three mutually perpendicular directions. Hence three measurement channels may be required to record vibration at any point. Up to the present, where vibration measurements have been required at a number of points, mechanical switches have been employed to switch in new sets of transducers manually during a particular run or else a number of runs have been performed to assemble the required amount of data. To overcome the above limitations a system for multiplexing and recording a number of data channels over a large bandwidth is proposed.

Because of the large bandwidth requirement of each of the multiplexed FM channels it is not possible (with the present recording equipment) to sample sufficiently fast to allow regeneration of the data from a series of sample points when reproducing. The only satisfactory way of multiplexing is to allocate time slots (relatively long compared with the period of the lowest frequency to be measured) for each measurement channel. With such a system exact time coincidence between the various data samples is not possible but a good improvement relative to present methods would be achieved. One of the main problem areas of such a multiplexing system is that of de-multiplexing the data when reproducing if a separate recording track is not used to record synchronizing information. In this regard it is envisaged that the digital time-of-day information will be used for allocating time slots when recording and will be used for data recognition when reproducing. A complete system of multiplexing and recording of data using FM techniques is currently under development.

A pulse duration modulation (PDM) recording capability is presently available (with the exception of a multiplexer). It is expected that this recording technique will find application in situations where the increase in information rates possible over the digital system represents a significant advantage.

Digital techniques will be employed for recording data (having relatively low frequency content) to high accuracy (0·1%). Serial type recording is proposed to meet most requirements and parallel type recording is proposed for special applications in which analogue recording is not required.¹ The system as originally envisaged employed non-return-to-zero-mark [NRZM] recording in which the tape is continuously saturated in either the positive or the negative sense, a change in polarity occurring every time a “one” is recorded.

Two tracks are used for the serial digital recording in NRZM, one for the data and one for odd parity checkbits. Use of “OR” logic when reproducing enables introduction of the clock signal essential for reading NRZM data.

Because NRZM recording requires two tracks for serial recording some consideration has recently been given to return-to-zero (RZ) recording which requires the use of only one track. In the RZ system the tape is normally demagnetized. When a “one” is recorded the magnetization along the tape changes from zero to saturation in one sense and back to zero again. When a “zero” is recorded the tape is saturated in the opposite sense. The RZ system is more susceptible to errors as a result of tape dropout (considerable loss in reproducing amplitude will result from tape dropout²) than the NRZM system. Thus both systems will be made available as alternatives, the appropriate selection depending on the requirements of each particular measurement application.

Each serial word has a period equal to 20 data bit durations. The first sixteen bits represent the information, the seventeenth is a dummy bit, the eighteenth is an even longitudinal parity checkbit and the last two bits represent an interword gap. For the NRZM system the interword gap is indicated by no change in magnetization on either the data or the lateral parity track, and for the RZ system the interword gap is indicated by zero magnetization of the tape without change.

Each data frame or record (equivalent to one complete scan of data) has a period equivalent to that of a fixed number of words. The number of words which constitute a record may be preset. Originally¹ it had been envisaged that records be made a maximum of 20 words
in length, but recently it has been decided that the recording equipment be arranged to accommodate records of up to 100 (presettable) words corresponding to analogue inputs and up to 3 (also presettable) words corresponding to digital inputs. Initially only 24 analogue multiplexer channels will be available but the system will be such as to allow for future expansion if required. To identify words each record is preceded by a gap equivalent to the duration of one word. To reduce the number of bits required per word, address information is not recorded, and hence a counting procedure (to be performed eventually by a digital computer) is required for individual channel identification.

The system of serial recording originally postulated employed a word rate of 1000 per second at a tape speed of 60 inches per second (ips) and proportionately lower rates at lower tape speeds. The following table indicates the number of records per second (at a tape speed of 1½ ips) for various record lengths.

<table>
<thead>
<tr>
<th>Words per Record</th>
<th>1</th>
<th>4</th>
<th>5</th>
<th>8</th>
<th>10</th>
<th>16</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Records per second at 1½ ips tape speed</td>
<td>31·25 (125 per 4 sec.)</td>
<td>7·8125 (25 per 4 sec.)</td>
<td>6·25 (25 per 4 sec.)</td>
<td>3·90625 (25 per 8 sec.)</td>
<td>3·125 (25 per 8 sec.)</td>
<td>1·953125 (25 per 16 sec.)</td>
<td>1·5625 (25 per 16 sec.)</td>
</tr>
</tbody>
</table>

The table indicates that the number of records per second tends to be inconvenient. Such an arrangement is undesirable when data are to be plotted as a function of time.

In a new arrangement, a word rate of 1024 per second at a tape speed of 60 ips (and proportionately lower at lower tape speeds) is to be employed. The following table is to be compared with the one above.

<table>
<thead>
<tr>
<th>Words per Record</th>
<th>1</th>
<th>4</th>
<th>5</th>
<th>8</th>
<th>10</th>
<th>16</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Records per second at 1½ ips tape speed</td>
<td>32</td>
<td>8</td>
<td>6·4 (32 per 5 sec.)</td>
<td>4</td>
<td>3·2 (16 per 5 sec.)</td>
<td>2</td>
<td>1·6 (8 per 5 sec.)</td>
</tr>
</tbody>
</table>

This provides a considerable advantage for plotting of data as a function of time. The change in maximum recording rate from 1000 words per second to 1024 words per second represents a very small increase in rate which can readily be accommodated. However, modification to the basic clock pulse generator is required to provide the new rates.
The arrangement originally proposed required three words in each frame to record run number, day-of-the-year and time-of-day information. Such an arrangement means that a relatively large proportion of time (particularly when records contain a small number of words) is devoted to the recording of data which is fixed (run number and day-of-the-year) or varying in a predictable manner (time-of-day). In the new system, run number, day-of-the-year and time-of-day information will be allocated one word per record only and four consecutive records will define a complete reading of these data. The following table indicates the word composition which has been adopted.

<table>
<thead>
<tr>
<th>Word Number</th>
<th>Bit Number</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15</td>
</tr>
<tr>
<td>W11</td>
<td>Identifier</td>
</tr>
<tr>
<td></td>
<td>1 1 x x x x x x x x x x x x x x x x</td>
</tr>
<tr>
<td>W21</td>
<td>Hours</td>
</tr>
<tr>
<td></td>
<td>1 0 x x x x x x x x x x x x x x 0 0</td>
</tr>
<tr>
<td>W31</td>
<td>Month of Year</td>
</tr>
<tr>
<td></td>
<td>0 1 x x x x x x x x x x x x 0 0 0 0</td>
</tr>
<tr>
<td>W41</td>
<td>Run Number</td>
</tr>
<tr>
<td></td>
<td>0 0 x x x x x x x x x x x x x x 0 0</td>
</tr>
</tbody>
</table>

* W31 etc. means WORD 1 OF RECORD 3 and so on. B0 to B15 represent bit positions.

The two bit identifier occupying bit positions B0 and B1 enables easy recognition of the data.

With the system indicated above one time reading would be provided every four records. For the new word rate indicated above the following table applies.

<table>
<thead>
<tr>
<th>Words per Record</th>
<th>1</th>
<th>4</th>
<th>5</th>
<th>8</th>
<th>10</th>
<th>16</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time readings per second at 1 1/2 ips tape speed</td>
<td>8</td>
<td>2</td>
<td>1.6 (8 per 5 sec.)</td>
<td>1</td>
<td>0.8 (4 per 5 sec.)</td>
<td>0.5 (1 per 2 sec.)</td>
<td>0.4 (2 per 5 sec.)</td>
</tr>
</tbody>
</table>

Since the word rate and the time-of-day clock signals are derived from the same master clock signal it is possible to interpolate to obtain intermediate time readings.

The fixed data and the time-of-day information which will be multiplexed digitally as indicated above constitute one of three digital inputs available. Another two 16-line inputs will be available for recording the outputs of digital transducers (e.g. shaft encoders used for the measurement of control surface position) and the like. If more digital inputs need to be recorded multiplexing over a number of data frames (similar to that used for the fixed data and the time-of-day data) may be readily performed.

NRZM recording only will be used for seven channel parallel digital recording. Data will be recorded on four tracks (say tracks 1 to 4), word and frame synchronizing signals will be
recorded respectively on tracks 5 and 6, and odd lateral parity checkbits will be recorded on track 7. Hence 4 longitudinal bit groups (or bytes) will be used to record one data word. The proposed recording format is indicated in the table below.

<table>
<thead>
<tr>
<th>Track</th>
<th>Second Last Word in Record</th>
<th>Last Word in Record</th>
<th>First Word in Next Record</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>x x x x x x x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>x x x x x x x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>x x x x x x x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>P P P P P P P P P P P P P P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>P P P P P P P P P P P P P P</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

x means a data bit which may be either 0 or 1.
P means an odd parity checkbit.

As may be seen from the above table the second consecutive recorded “one” on track 5 indicates the end of a word and the fourth consecutive recorded “one” on track 6 indicates the end of a record. Hence for the parallel system of recording, digital techniques may be employed to recognize the end of a word and the end of a record.

3. REDUCTION OF DATA RECORDED USING ANALOGUE TECHNIQUES

The tape machine to be used for recording data by means of direct, FM and possibly PDM techniques is basically a record-only type which cannot conveniently be adapted for reproduction purposes. Hence the first requirement for the ground station data reduction equipment is that of an analogue reproducer. To this end a commercially available seven-channel analogue reproducer designed to handle direct, FM and PDM data has been acquired. To assist analysis of data using commercial spectral analysis equipment (also available at these laboratories) a tape loop adaptor capable of handling tape loops up to about 100 foot in length has also been acquired.

The speed of the reproducing machine capstan can be servo controlled using the recorded reference frequency. As the reference frequency will be recorded together with speech on a single direct recording channel appropriate circuits have been developed to separate these signals.

FM demodulation will be readily performed by “plug-ins” which are available for use in the analogue reproducer. Analysis procedures to be used with the demodulated FM data vary according to the particular measurement application. However, one area of prime importance is the measurement of amplitudes and frequencies of the various signal components. At the present time the measurements are made with spectral analysis equipment which is controlled manually. Later on this equipment will be controlled automatically by signals received from a digital computer.

Reduction of the multiplexed FM data is complicated by the synchronization requirements. If time slots derived from the real time recording clock are used then synchronizing signals may be derived from the digital data processing equipment used to reduce the digital data (Sec. 4.3).

Reduction of data recorded using FM techniques will often be done with the aid of a digital computer. Programmes are available for spectral analysis in this way. Since frequencies as high as 10 kilohertz may be included a high speed analogue to digital converter will be required. Assuming 10 samples are required per cycle of the maximum frequency then \(10^6\) samples are required per second for each data channel. If 8-bit words are used (providing a resolution of 1 part in 255 which should be adequate for this data), then \(8.10^6\) bits of information must be read per second if the data are reproduced at the same tape speed as used for recording.

7
Since the number of data bits required per second may exceed computer handling capabilities it may be desirable in some instances to reproduce at a lower speed than that used for recording. The effective data rate halves for each speed reduction step. The reduction in tape speed may overcome the limitations due to inadequate computer speed. However, another problem is that of data storage. Since sufficient time may not be available for detailed reduction, a capability for re-recording the data without intermediate computation on some bulk storage unit such as a magnetic tape unit is thought to be best in this case. Later analysis may be performed either at a lower data rate or with a high speed computer having a large storage capacity.

Possible methods of reducing PDM data have already been discussed.\(^1\) It is envisaged that most reduction will be performed with the aid of a digital computer.

4. REDUCTION OF DATA RECORDED USING DIGITAL TECHNIQUES

4.1. General Requirements

As indicated in Sec. 2 the recorded digital data may be in any one of the following forms:

(i) NRZ on two tracks (one track for data and one for odd lateral parity);
(ii) RZ on one track;
(iii) NRZ on seven tracks.

(i) and (ii) are recorded together with analogue quantities using staggered analogue heads in accordance with IRIG\(^4\), whereas (iii) is recorded using a single in-line digital head. In each case the recording is not in computer compatible format and, as such, cannot be read directly into a digital computer using a conventional magnetic tape interface. Because of the need for time correlation between data recorded using analogue techniques and data recorded using digital techniques it is essential that digital data recorded in (i) or (ii) be read using the analogue tape reproducing machine referred to in Sec. 3. Digital data recorded in (iii) may also be read using the same analogue reproducer but the pair of staggered analogue reproducing heads would need to be replaced with a single in-line digital head.

A block schema of the proposed data processing system is shown in Fig. 1. Processing of data, recorded using either digital or analogue techniques, with a digital computer, is indicated. The processing of analogue data using analogue reduction equipment is indicated as an alternative.

A model PDP-10 digital computer manufactured by Digital Equipment Corporation is available at these laboratories for processing digital data. Normally this computer is operated simultaneously by a number of users in a time shared mode. If the digital data, referred to earlier, were read on-line by this computer after suitable interfacing (without memory), operation of the PDP-10 in the normal time shared mode would not be possible as data reproduced by an analogue machine cannot "wait." Another difficulty associated with on-line operation is the need for relatively large special purpose equipment (e.g. analogue reproducer and digital interface equipment) in the very limited space available in close proximity to the PDP-10. This latter difficulty would not apply if the data were transmitted via land lines from a remote location. However, at the high data rates involved (up to \(10^9\) 16-bit words per second for data recorded using digital techniques and possibly up to \(10^8\) 8-bit words per second for data recorded using analogue techniques) an installation costing more than a small self-contained data processor would be needed. For these reasons it has been decided that a small data processing facility be provided which may be located remotely from the PDP-10 and which will provide a computer compatible tape suitable for further processing with the PDP-10. In this way processing of the required data with the PDP-10 may "take its turn" in the queue.

In order to produce a computer compatible tape, some buffer storage and a digital magnetic tape unit are required. Small digital computers provide a very convenient buffer storage and can be readily programmed to read data out in appropriate form into a magnetic tape unit (Fig. 1). An additional advantage of using a small digital computer for this is that it may be used for processing data in its own right. Because of the large volumes of recorded data involved and because of a very high demand on readout equipment the ability to do at least some processing away from the PDP-10 is highly desirable. In many instances relatively simple computations will be required on large volumes of data (a requirement readily accommodated by a small digital computer). Readout of data will normally be via a printer or an incremental plotter.
One of the readout requirements will be the plotting of data (as recorded or computed) as a function of recorded time. Since time is recorded digitally it may be used to increment the plotter. The more involved processing which will be required can be performed by the PDP-10.

Because of the serial nature of the recorded digital data some re-arrangement is required before it is read by a digital computer. Data words [recorded in forms (i), (ii) or (iii) mentioned earlier] effectively contain 16 information bits and one longitudinal parity bit. Many of the small computers will read 16-bit words directly. It has been decided that the data be arranged in 16-bit parallel words using digital interface equipment. In addition parity checkbits will be generated. Since the data rate is set by the analogue reproducer it is essential that the digital computer read the 16-bit parallel input at the appropriate times. Most digital computers will accept read commands and hence the interface equipment should also provide these. The digital interface equipment (Fig. 1) is currently under development.

Another requirement of the digital interface equipment is that it read and display the run number and day-of-the-year information required for record identification, and the time-of-day information required for identifying any areas of interest on the tape. It must be possible to stop the analogue reproducing machine at any pre-selected time.

In order to process the data using a small digital computer (or the PDP-10) suitable software is required. Normally the programmes would be written on paper tape and read into the computer with the aid of a high speed reader (Fig. 1). Since the programme requirements represent a relatively large area of investigation they have been made the subject of another paper to be published later.

4.2. Analogue Reproducing Machine Requirements

As stated in Sec. 4.1 digital data recorded in either serial or parallel form will be reproduced using an analogue machine. Usually reproduced signals are taken to suitable plug-in conditioners which provide outputs virtually identical to the signals at the corresponding inputs to the analogue recording machine at the time of recording.

In the case of the currently available analogue machine (an Ampex Model FR1260) the manufacturer does not supply any digital reproducing conditioners. For this reason, and also because digital reproducing conditioners are required for use in a field monitor unit (which enables a "quick look" to be obtained at data recorded by the airborne magnetic tape recorder) some digital reproducing conditioners have been developed at these laboratories.

For NRZM type recording the tape magnetization takes the form indicated in Fig. 2(b). The signal received from the reproducing head is first amplified using a linear preamplifier and then taken to the NRZ reproducing conditioner. The pre-amplifier output signal waveform is indicated in Fig. 2(c).

Reproducing head signal level is very closely proportional to reproducing speed (irrespective of the speed of recording). Since one of the basic requirements of the serial system is that reading of data be possible at any tape speed (between 1 3/4 ips and 60 ips), it is essential that the conditioner accommodate the variations in reproducing head signal arising at different tape speeds. To obtain reasonable immunity from noise either a switched gain amplifier (gain approximately inversely proportional to tape speed) or an amplifier incorporating automatic gain control can be employed. At the present time a switched gain amplifier is used but an investigation of an amplifier incorporating automatic gain control is scheduled.

The block schema of Fig. 3 indicates in general terms the operating principle of the NRZ reproducing conditioner. The pre-amplifier output signal is first passed to an amplifier the gain of which is varied according to tape speed. Since in NRZM recording a change of magnetization in either direction must be read as a "one" the output of the variable gain amplifier is full wave rectified. In order to regenerate a NRZM output waveform a trigger circuit is used to convert from the relatively slow waveform of the full wave rectifier to a fast output waveform required for triggering the output flip-flop. Each of the blocks of Fig. 3 will now be examined in detail.

In Fig. 4 full circuit details of the NRZ reproducing conditioner are given. For information on the system of component identification and the method of indicating component values used here and elsewhere throughout the text refer to Appendix 1.

For data recorded in NRZ form, the reproducing pre-amplifier output typically varies from 80 millivolt (peak to peak) at a tape speed of 1 3/4 ips to about 2 0 volt at 60 ips. Amplifier Q1 of the NRZ reproducing conditioner (Fig. 4) is arranged to provide gain inversely proportional
to the tape reproducing speed. High frequency attenuation, the cut-off frequency of which is closely proportional to tape reproducing speed, is provided by C2 connected in shunt across the gain determining feedback resistor. Adjustment of gain at all tape reproducing speeds is made possible by use of a single potentiometer R11.

Transistors Q2 and Q3 and associated components effectively rectify the variable gain amplifier output signal and provide a series of positive pulses at the collector of Q3 corresponding to recorded “ones.” Adjustment of R20 allows output pulses arising from positive excursions of the amplifier output to be made equal in amplitude to those arising from negative excursions.

In order to reject noise and provide an output having fast rise-time (required for clocking of series 7400 flip-flops) a form of Schmitt trigger circuit incorporating Q4, Q5A, Q5B and associated components is used. The resultant negative-going trigger pulse has short rise and fall times (less than 20 nanosecond) which are very nearly independent of the slope of the incoming waveform.

The output flip-flop Q6 switches in synchronism with the leading edges of the trigger circuit output. Q5C acts as a buffer to isolate the output of flip-flop Q7 from the co-axial line connecting the NRZ output of this conditioner to the digital interface (Sec. 4.3). A NRZ output switching between standard TTL (transistor-transistor-logic) levels is provided.

For the serial system in which NRZM data is recorded on one track and odd parity (also in NRZM) is recorded on another track two conditioners of the type indicated in Fig. 4 are required. Similarly seven of the same conditioners may be used for regenerating the NRZM data in the 7-channel parallel recording system.

In RZ type recording a “one” is recorded as an excursion from zero tape magnetization to positive saturation and back to zero again whereas a “zero” is recorded as an excursion of the opposite polarity. For the RZ recording system which has been adopted the recording head current takes the form of positive or negative pulses of 5 microsecond duration at all tape speeds. The use of constant and relatively short duration pulses over the complete range of tape speeds is justified as the recorded wavelength approximates a recording head gap width at all tape speeds (provided the distance moved by the tape over the duration of the head current pulse is small compared with the gap width. Eldridge, Stein and Barkouki analyse the pulse recording process and indicate how the characteristics of the reproducing pulse may be evaluated.

On reproducing the recorded RZ data the reproducing pre-amplifier output signal takes the form indicated in Fig. 2(e). A recorded “one” is reproduced as a pair of pulses consisting of a positive peak followed by a negative peak, and vice versa for a recorded “zero.” The peak to peak amplitude of the reproducing pre-amplifier output varies typically from about 65 millivolt at a reproducing speed of 1½ ips to 1500 millivolt at a reproducing speed of 60 ips for data recorded on an Ampex Model AR200 (used for the airborne recording) and reproduced on an Ampex Model FR1260. The output amplitude is approximately proportional to reproducing speed. On reproducing RZ data the duration of a pulse pair corresponding to a “one” or a “zero” (recorded using the Ampex Model AR200) varies from 800 microsecond approximately at 1½ ips to 30 microsecond approximately at 60 ips and is very nearly inversely proportional to the reproducing speed.

Data recorded in RZ form needs to be handled using a different conditioner to that used for the NRZ data.

The block schema of Fig. 5 indicates in general terms the operating principle of the RZ reproducing conditioner. The pre-amplifier output signal is first passed to an amplifier the gain of which is varied according to tape speed. Positive excursions of the variable gain amplifier output are converted via a Schmitt trigger circuit into a train of pulses with short rise and fall times, and similarly negative excursions of the variable gain amplifier output are converted via another Schmitt trigger circuit into another train of pulses on a separate output. The two pulse trains (P and N) are first converted to a NRZC (non-return-to-zero-charge) output, then to a NRZ1 output (normal NRZM output) and a NRZ2 output (NRZ output with changes corresponding to recorded zeros). Each of the blocks of Fig. 5 will now be examined in more detail. In Fig. 6 full circuit details of the RZ reproducing conditioner are given.

The pre-amplifier output signal (Fig. 2(f)) is amplified by a variable gain amplifier (comprising Q51 and associated components) similar to the one used for the NRZ data. In this
instance however the amplifier has broader bandwidth since inadequate bandwidth will result in severe distortion due to relative phase shift of the signal components.

A pair of Schmitt trigger circuits (similar to the one used for the NRZ data) produces two series of pulses corresponding respectively to positive and to negative excursions of the preamplifier output. These are marked respectively as P and N in Fig. 6. The P and N signals are normally in the “one” state but switch to “zero” state for the duration of the respective Schmitt output pulses.

As indicated in Fig. 2(f) two consecutive positive pulses indicate a change from a recorded “zero” to a recorded “one” and two consecutive negative pulses indicate a change from a recorded “one” to a recorded “zero.” Such changes of state may be readily detected using digital circuits only (after suitable conditioning with the Schmitt circuits). Since changes of state in the recorded data are guaranteed (introduced in format used for recording fixed data and time-of-day) the detection of these is employed as the basis on which the reproduced data is decoded.

In Figs. 2(g) and 2(f) the Schmitt output signals P and N have been drawn. The times corresponding to the leading and the trailing edges of the first of each pair of pulses have been designated T1 and T2 respectively and the times corresponding to the leading and the trailing edges of the second of each pair of pulses have been designated T3 and T4 respectively.

Changes of state are detected using flip flop Q56A and associated components. Flip flop Q56A is preset (Q output set to the “one” state) on the trailing edges of the N pulses and is cleared (Q output set to the “zero” state) on the trailing edges of the P pulses. The outputs of the inverters Q52E and Q52F are normally in the “one” state by virtue of the input resistors R77 and R78 but switch to the “zero” state for a duration of about 300 nanoseconds when P or N respectively switch from the “zero” to the “one” state. If a change of state from a “zero” to a “one” occurs two P pulses will arrive without a N pulse in between. On the arrival of the second P pulse the output Q of flip-flop Q56A will be in the “zero” state and a “one” level pulse will be propagated to the K input of flip flop Q59. Similarly if a change of state from a “one” to a “zero” occurs a “one” level pulse will be propagated to the J input of flip flop Q59. Clocking of Q59 is provided by way of NOR gate Q57C which causes the J-K input data to be transferred to the output about 300 nanoseconds after either the J or the K input switches to the “one” state. The output of Q59 is effectively in NRZC format (a non-return-to-zero output which changes state each time a change in bits occurs) but with the special property that the direction of change indicates the actual bit change which has occurred.

Flip flop Q56B generates a clock signal which enables the NRZC output to be read. Whenever a change of bits occurs a clear pulse of about 300 nanosecond duration starting at T1 is coupled through the NOR gate Q57C to this flip flop and checks that the Q output is in the “zero” state. The P and N signals are inverted using NAND gate Q58A and are then taken to the clock input of flip-flop Q56B. At time T2 the Q output of flip flop Q56B switches to the “one” state and at time T4 it switches back to the “zero” state.

Using the NRZC output of Q59 and the clock output of Q56B two channels of NRZ data are generated by Q60. The NRZ1 output of Q60B changes state each time a “one” is reproduced and the NRZ2 output of Q60A changes state each time a “zero” is reproduced. The NRZ outputs always change state at T3 as indicated in Figs. 2(i) and 2(j).

Q58B and Q57D act as buffers for the outputs of flip flops Q60A and Q60B so that these will not be loaded by co-axial output lines.

The two channels of NRZ data produced by the RZ conditioner have been chosen in preference to a single channel of RZ data (similar to the corresponding input of the airborne magnetic tape recorder) as the outputs are then identical to those produced for the two-channel NRZ system. Hence using a RZ reproducing conditioner of the type described, the digital interface equipment (Sec. 4.3) need handle only NRZ data.

4.3. Digital Interface

Basically the digital interface is required to:

(i) Arrange the digital data into 16-bit parallel words for reading into a digital computer.
(ii) Display run number, month-of-the-year, day-of-the-month and time-of-day information.
(iii) Provide a control signal which will enable the analogue reproduce tape transport to be stopped at any preset time.
The various functions performed within the digital interface are indicated in the block schema of Fig. 7. These functions will now be considered separately.

4.3.1. Input Clock Signal Generator

The outputs of the reproducing signal conditioners (Sec. 4.2) constitute the inputs to the digital interface. In the case of data recorded serially either in NRZM format on two tracks (one track for the data and one track for odd parity checkbits) or in RZ format on one track, the outputs of the appropriate reproducing conditioners take the form of two channels of NRZ data (the first providing level changes for recorded “ones” and the second for recorded “zeros”). In the case of data recorded in seven channel parallel form using NRZM techniques the outputs of the reproducing conditioners are likewise in NRZM format. Hence all inputs to the digital interface are in NRZM format.

The NRZM inputs are taken to the input clock signal generator (Fig. 1) which converts the level changes associated with the NRZM data into negative going clock pulses (i.e. a signal which is normally high [“one” level] but which switches low [“zero” level] for the duration of the pulses).

For data recorded serially the following are generated:

(i) Clock pulses \( A_4 \) corresponding to recorded “ones.”
(ii) Clock pulses \( A_2 \) corresponding to recorded “zeros.”
(iii) Clock pulses \( A \) corresponding to recorded “ones” or “zeros” where \( A = A_1A_2 \).

A circuit diagram for the input clock signal generator for the serial system is shown in Fig. 8. Inverters Q101A and Q101C improve input signal rise times which may have been degraded somewhat in passing from the reproducing signal conditioners to the digital interface via co-axial cables. The inputs to each of the NOR gates Q102A and Q102B are normally low but when a transition on one of the NRZ inputs takes place a positive pulse will be capacitively coupled to one of the NOR gate inputs thus switching the output of that gate low. Pulse duration is defined by the coupling network comprising C101 and R101 etc. which in this case has been set to provide 4 microsecond pulses approximately. The outputs of the NOR gates Q102A and Q102B constitute the \( A_1 \) and \( A_2 \) clock signals respectively. Generation of the logical AND function \( A_1A_2 \) (designated by \( A \)) is provided by Q101E, Q101F and Q102C.

For data recorded in parallel the following are generated (Fig. 9):

(i) Clock pulses corresponding to recorded “ones” on each track \((A_1 \text{ to } A_7)\).
(ii) Clock pulses corresponding to the logical AND function \( A_1A_2A_3A_4A_5A_6A_7 \) (designated by \( A \)).

The circuit of the input clock signal generator for the parallel system (Fig. 9) is similar to that for the serial system; pulse durations are the same. Since the data has not been “deskewed” at this stage it is possible to obtain more than one pulse per byte (a parallel sample of data containing seven bits). Moreover it is possible to extend the pulse duration beyond the nominal value (set by the coupling network C151 and R151 etc.) due to the time delays between input transitions.

4.3.2. Electronic Flywheel

For data recorded serially (either utilizing two channels of NRZM or one channel of RZ) each word is composed of 16 information bits (in some cases the effective words are shorter and unused bits are recorded as zeros), one longitudinal parity bit, one dummy bit and a space of two bit durations constituting an end-of-word (EOW) gap. The number of words per data frame (or record) may be set anywhere in the range 2 to 100 by the recording equipment. At present the recording equipment will accommodate only 24 channels of multiplexed analogue data (subsequently converted to digital form with an analogue to digital converter) and hence the upper limit generally does not exceed 25 channels after due allowance for an additional digital input providing the time-of-day and fixed information (Sec. 2).

Each data frame is followed by an end-of-record (EOR) gap having a duration equivalent to that of one word plus an EOW gap. Hence a gap of effectively 22 bit durations occurs at the end of each data frame. To read the reproduced digital data it is essential that the interface equipment detect both the EOW and the EOR gaps.

A gap (either an EOW or an EOR) is characterized by no level change on either the data channel or the odd parity channel for the two channel NRZM system or by zero magnetization
without change for the RZ system. In the following table the bit repetition period, the EOW gap duration and the EOR gap duration are given for the various tape speeds assuming a bit rate of 20-48 kilohertz is adopted at 60 ips tape speed and proportionately lower rates are used at lower tape speeds.

<table>
<thead>
<tr>
<th>Tape Speed (ips)</th>
<th>Bit Duration (microseconds)</th>
<th>EOW Gap Duration (microseconds)</th>
<th>EOR Gap Duration (microseconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>48.8</td>
<td>97.6</td>
<td>1074</td>
</tr>
<tr>
<td>30</td>
<td>97.6</td>
<td>195.3</td>
<td>2148</td>
</tr>
<tr>
<td>15</td>
<td>195.3</td>
<td>390.6</td>
<td>4297</td>
</tr>
<tr>
<td>7.13</td>
<td>390.6</td>
<td>781.3</td>
<td>8594</td>
</tr>
<tr>
<td>3.47</td>
<td>781.3</td>
<td>1562.5</td>
<td>17188</td>
</tr>
<tr>
<td>1.75</td>
<td>1562.5</td>
<td>3125.0</td>
<td>34375</td>
</tr>
</tbody>
</table>

As indicated in the above table bit duration, EOW gap duration and EOR gap duration have been made inversely proportional to tape speed.

Gap detection considerations apply only to the serial system of recording as gaps are not employed for the parallel system. A convenient input to a gap detection system is the A output of Fig. 8 (see also Sec. 4.3.1) which provides negative going (i.e. a signal normally in the "one" state but switching to "zero") clock pulses of nominally 4 microsecond duration for each recorded "one" or "zero." EOW and EOR gaps are indicated by the absence of clock pulses in the A output. Recognition of EOW or EOR gaps involves the use of analogue techniques since a gap is, in effect, a time interval in which no digital recording of bits takes place. Various techniques may be used for gap detection; some of these will now be discussed.

In the simple system depicted in Fig. 10 the input clock pulses A reset a linear ramp circuit. Hence the peak ramp voltage attained for any given time interval between pulses will be proportional to that interval (assuming the ramp circuit is not driven into a non-linear region of operation). Using voltage comparators to compare ramp voltage level with preset reference levels enables EOW and EOR pulses to be generated (Fig. 10b). To enable the gaps to be detected at all reproducing speeds, manual switching of ramp slope so as to make this parameter proportional to tape speed is required (assuming the bit repetition rate is also made proportional to tape speed). For brevity the system described here will be referred to as the "simple" system in what follows.

In the system depicted in Fig. 11 a relaxation oscillator (e.g. astable multibrator, sawtooth generator etc.) is adjusted so that it has a free-running period a little greater than that of the incoming clock repetition period. Whenever a series of clock pulses is delivered to the input the oscillator will be triggered such that its period locks on to that for the incoming clock. In the absence of input clock pulses, the oscillator will revert to the free-running mode of operation. The output of the oscillator is capacitively coupled to an inverter to provide short duration negative going output pulses (Fig. 11b). These pulses are produced in synchronism with the incoming clock when clock pulses are present and are produced as determined by the free-running period of the oscillator when pulses are absent. By making the duration of these output pulses shorter than that of the input clock pulses, the pulses inserted during the gaps may be readily separated. The output clock pulses may be inverted and taken together with the input clock pulses to a NAND gate to provide the required inserted clock output. The number of inserted pulses which arrive between successive input clock pulses can be readily counted using digital techniques. Hence EOW gaps (indicated by two successive inserted clock pulses) and EOR gaps (indicated by a number in excess of two inserted clock pulses, say 9) may be readily detected. To enable the gaps to be detected at all reproducing speeds manual switching of the free-running period of oscillation so as to make this parameter inversely proportional to tape speed is required. Because of the need for manual switching of the free-running period when reproducing speed is changed this system will be referred to in what follows as the "semi-automatic" system to distinguish it from the fully automatic system to be described below.

There are some distinct advantages of the semi-automatic system over the simple system. One of the main advantages is that clock pulses would be inserted if an input clock pulse were
missed due to tape dropout or other cause. Hence errors can be confined to the bit corresponding to the missing input clock pulse and a complete displacement of bits does not take place as would occur for the simple system. If the free-running oscillator is so arranged that triggering can only occur over a portion of the incoming clock repetition period then increased immunity to noise, which may produce extraneous additional clock pulses, would result. However, to enable this latter performance to be realized some oscillation inhibit would be required, after a certain number of inserted clock pulses in the EOR gap have been counted, to ensure that the oscillator triggers on the first clock pulse which arrives after an EOR gap.

The system of gap detection depicted in Fig. 12 is a fully automatic system and will be called an “electronic flywheel” because of the analogy to a mechanical flywheel. Basically the mechanical flywheel will tend to maintain a steady rotational speed even if the applied driving torque is interrupted. Irrespective of the actual speed of rotation of the flywheel it will always react so as to maintain that speed. If while the flywheel is rotating the driving torque is reduced to and maintained at zero the flywheel will gradually slow down at a rate determined by the inertia of the flywheel and associated rotating members and the output torque.

In a similar manner the electronic flywheel will insert pulses (analogous to mechanical rotations) whenever the source of incoming pulses is interrupted and the repetition period of the inserted pulses will be automatically adjusted close to that of the incoming pulses. If the incoming pulses are stopped the repetition period of the free oscillations will gradually increase.

In the flywheel system depicted in Fig. 12 incoming clock pulses pass through the NAND gate and reset the fixed slope ramp generator output to zero. Hence when pulses are applied, the repetition period of the ramp voltage waveform will be adjusted to that of the incoming clock. The ramp output is taken to a peak charging circuit which converts the ramp voltage peaks (proportional to input clock repetition period) into a steady output signal (also proportional to input clock repetition period). The ramp output is attenuated and compared with the output of the charging circuit. When input clock pulses are applied, the comparator (Fig. 12) does not switch. However, if the input clock pulse train is interrupted, the comparator will switch and send back pulses which reset the ramp output to zero. Hence in the temporary absence of incoming clock pulses the ramp will free-run with a repetition period somewhat longer than that of the input clock (Fig. 12).

The electronic flywheel has the particular advantage that it will handle data rates which may vary continuously over a wide range (in this case a data rate varying in the range 1 to 32 times the minimum rate) without the need for switching or adjustment of any components. Just as in the case of the semi-automatic system, a clock pulse will be inserted if an input clock pulse is missed due to tape dropout or other cause.

By adding some additional features to the electronic flywheel, increased noise immunity will result as in the semi-automatic system. As will be shown later these features make the system ideal also for use in the parallel system of recording for which only one output clock pulse is permitted per byte. Due to the inherent skew of the parallel data more than one input clock pulse is possible per byte (Sec. 4.3.1).

The electronic flywheel has been adopted for use in the digital interface because of the distinct advantage mentioned above. Due to the novel nature of the electronic flywheel and because of its wide range of possible applications the operational features will now be examined in more detail.

A block schema of the complete electronic flywheel as used in the digital interface is drawn in Fig. 13 and complete circuit details are given in Fig. 14. Some features additional to those shown for the basic system of Fig. 12 are indicated.

To establish a constant time interval during which the ramp generator is reset, a delayproducing monostable multivibrator (subsequently referred to as a “delay monostable” or as a “monostable”) has been used. It is essential that sufficient reset time be provided to allow the ramp capacitor C203 to completely discharge through Q203 during this time. Normally at the time of arrival of input clock pulses A, the levels at E and F (Figs. 13 and 14) are high (“one” state) and the delay monostable is triggered on the negative going transitions of the A pulses where an A pulse is indicated by a change from a high to a low level for a time duration of about 4 microsecond (Sec. 4.3.1). The delay provided by the monostable has been set to 1.4 microsecond approximately which is short compared with the lowest bit repetition period of interest (48.8 microsecond at 60 ips tape speed). As will be indicated later negative going clock pulses E of
relatively short duration are generated during the EOW and EOR gaps and are fed back to the delay monostable input. These pulses, like the A pulses, trigger the monostable on the negative going transitions. A deskewed clock signal F (to be discussed later) is fed back to the monostable to prevent the latter from being triggered until a certain proportion of a bit repetition period has elapsed since the arrival of the last A or E pulse.

The ramp generator (Fig. 14) utilizes a conventional bootstrap sweep arrangement with emitter follower output to prevent loading of the ramp charging circuit. Ramp slope is determined approximately by the supply rail voltage (+15 volt) divided by the product of R205 (100K) and C203 (33K) where (as elsewhere in this paper) resistance values are given in ohm and capacitance values are given in picofarad. Hence a slope of approximately 4·5 volt per millisecond is provided. In the following table the approximate peak ramp voltage excursion is given as a function of the bit repetition period (interval between input clock pulses) for the various tape speeds.

<table>
<thead>
<tr>
<th>Tape Speed (inch per second)</th>
<th>Bit Repetition Period (microsecond)</th>
<th>Peak Ramp Output (volt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>48·8</td>
<td>0·22</td>
</tr>
<tr>
<td>30</td>
<td>97·6</td>
<td>0·44</td>
</tr>
<tr>
<td>15</td>
<td>195·3</td>
<td>0·88</td>
</tr>
<tr>
<td>7½</td>
<td>390·6</td>
<td>1·76</td>
</tr>
<tr>
<td>3½</td>
<td>781·3</td>
<td>3·51</td>
</tr>
<tr>
<td>1¾</td>
<td>1562·5</td>
<td>7·03</td>
</tr>
</tbody>
</table>

The ramp output is reset to zero by the output NAND gate Q202A which inverts and provides buffering for the delay monostable output D. Note that D constitutes the output clock and includes clock pulses corresponding to both the input clock A and the inserted clock E.

To generate a steady voltage proportional to the average repetition period of the output clock a peak charging circuit is used. An average detecting circuit could have been used in this application but the output would be lower.

A simplified version of the peak detector used is illustrated in Fig. 15a. When the ramp voltage approaches its peak value CR2 will conduct and the charge lost by the capacitor since the previous ramp peak occurred, will be replenished. At the same time CR1 will also be in a state of conduction and ideally the two diode voltage drops will cancel giving a peak output from the detector (prior to discharge) equal to the peak value of the ramp input voltage. In order to charge the capacitor at the required rate of 4·5 volt per millisecond a charging current of 4·5 milliamp per microfarad of capacitance is needed. To provide the required charging current and at the same time reduce the loading on the ramp output a transistor (Q206 of Fig. 14 or Q1 of Fig. 15b) has been used in place of CR2 (Fig. 15a). Ideally, once again, the voltage drop across CR1 of Fig. 15b (CR202 of Fig. 14) should cancel with the emitter-base forward voltage drop of Q1 in Fig. 15b (Q206 of Fig. 14). However, due mainly to current differences in CR1 and Q1 the respective voltage drops will only cancel approximately. Note that CR203 (Fig. 14) is used only for voltage protection of the comparator to which the ramp is connected.

Two important additions have been incorporated in the circuit of Fig. 15b (also Fig. 14). In the first instance resistor R3 (R209 of Fig. 14) has been returned to the negative supply rail rather than to the common terminal. As a consequence the ratio of maximum to minimum ripple voltage across C1 (C204 of Fig. 14) for the full range of ramp inputs is reduced and improved linearity in the relationship between the output of the peak detector and the peak value of the ramp input results. It is essential that a reasonable level of ripple be developed across C1 otherwise circuit response would be too slow. In the second instance further filtering by way of R2 (R210 of Fig. 14), R3 (series connection of R212 and R213 of Fig. 14) and C4 (C205 of Fig. 14) has been included to enable a smoothed output proportional to the peak value of the ramp input to be obtained. This latter filtering is essential to the operation of the electronic flywheel as the output across C2 must not follow any rapid voltage changes across C1 but must only respond to changes in average value. If C2 were removed the output across R3 would follow the voltage changes across C1 and the comparator would never trigger.
Because the performance of the peak charging circuit has a very important bearing on the overall flywheel performance a simplified analysis of this circuit will now be carried out. Define the following with reference also to Fig. 15b:

- \( v_1 \) is the instantaneous voltage drop across \( C_1 \).
- \( V_1 \) is the peak value of \( v_1 \) corresponding to the peak value of ramp input.
- \( v_2 \) is the instantaneous voltage drop across \( C_2 \) (i.e. the output voltage).
- \( V_2 \) is the average value of \( v_2 \).
- \( i \) is the instantaneous discharge current through \( C_1 \).
- \( i_0 \) is the initial value of \( i \) at the beginning of the discharge of \( C_1 \).
- \( V_{cc} \) is the negative supply voltage.

At the lowest ramp frequency of interest (approximately 640 hertz) the ripple attenuation from \( v_1 \) to \( v_2 \) (considering the fundamental component only) may be found by substituting \( \omega = 2\pi \cdot 640 \) radian per second in

\[
\frac{v_2}{v_1} = \frac{R_3}{(R_2 + R_3)\left(1 + \frac{j\omega C_2 R_3}{R_2 + R_3}\right)}
\]

Hence substituting component values indicated in Fig. 15b we obtain

\[
\frac{v_2}{v_1} = \frac{0.017 R_3}{R_2 + R_3}
\]

\[
= 0.017. \text{(attenuation for average component)}
\]

Therefore it may be assumed that the output voltage across \( C_2 \) will to a good approximation remain static over a period of the ramp input voltage. In calculating the voltage across \( C_1 \) it will be assumed that a steady voltage \( V_2 \) is present across \( C_2 \) (i.e. \( v_2 = V_2 \)).

With reference to Fig. 15b we may write

\[
i = \frac{v_1 + V_{cc}}{R_1} + \frac{v_1 - V_2}{R_2}
\]

\[
i = \frac{R_1 + R_2}{R_1 R_2} v_1 + \frac{V_{cc}}{R_1} - \frac{V_2}{R_2}
\]

(1)

Hence

\[
\frac{dv_1}{dt} = \frac{R_1 R_2}{R_1 + R_2} \frac{di}{dt}
\]

Also

\[
\frac{dv_2}{dt} = -i
\]

Therefore

\[
\frac{R_1 R_2}{R_1 + R_2} \frac{di}{dt} = -C_1
\]

\[
i = i_0 \exp\left(-\frac{t(R_1 + R_2)}{C_1 R_1 R_2}\right)
\]

(2)

where \( i = i_0 \) at \( t = 0 \) and defining \( t = 0 \) at the instant the peak voltage \( V_1 \) is reached across \( C_1 \) we may write using (1):

\[
i_0 = \frac{R_1 + R_2}{R_1 R_2} V_1 + \frac{V_{cc}}{R_1} - \frac{V_2}{R_2}
\]

Substituting for \( i_0 \) in (2) we obtain

\[
i = \left(\frac{R_1 + R_2}{R_1 R_2} V_1 + \frac{V_{cc}}{R_1} - \frac{V_2}{R_2}\right) \exp\left(-\frac{t(R_1 + R_2)}{C_1 R_1 R_2}\right)
\]

Now

\[
v_1 = V_1 - \frac{1}{C_1} \int_0^t i \, dt
\]

\[
= V_1 - \left(V_1 + \frac{R_2}{R_1 + R_2} V_{cc} - \frac{R_1}{R_1 + R_2} V_2\right) \left(1 - \exp\left(-\frac{t(R_1 + R_2)}{C_1 R_1 R_2}\right)\right)
\]

(3)
For small $t$, $\exp\left(-\frac{t(R_1 + R_2)}{C_1R_1R_2}\right)$ may be approximated by $1 - \frac{t(R_1 + R_2)}{C_1R_1R_2}$.

Such an approximation is valid over a time interval equal to the period between successive input clock pulses. Hence equation (3) becomes

$$v_1 \approx V_1 - \left(V_1 + \frac{R_2}{R_1 + R_2} V_{cc} - \frac{R_1}{R_1 + R_2} V_2\right) \frac{R_1 + R_2}{C_1R_1R_2} t$$

(4)

Differentiating we may find the slope ($k_d$) of $v_1$ on discharge

$$k_d = \frac{dv_1}{dt} = -\frac{V_{cc}}{C_1R_1} - \frac{(R_1 + R_3)}{C_1R_1R_2} \left(V_1 - \frac{R_1}{R_1 + R_2} V_2\right)$$

(5)

Now $V_2$ defines the average output voltage and is related to the previous time history of the input voltage $v_1$. For a continuous input clock (no time gaps requiring pulse insertion) the value of $V_2$ will not change with time. Actually $V_2$ will vary with $k_d$ but to obtain a reasonable approximation to $k_d$ it can be assumed that

$$V_2 \approx \frac{R_3}{R_2 + R_3} V_1$$

Substituting this value of $V_2$ into equation (5) we obtain

$$k_d \approx -\frac{V_{cc}}{C_1R_1} - \frac{V_1}{C_1R_1(R_3 + R_2)} \frac{1}{R_1 + R_2 + R_3}$$

(6)

Hence the discharge slope may be considered to be the summation of a constant slope and a slope which varies with the peak input voltage $V_1$. For the component values used (Fig. 15b) the constant term is 0.71 volt per millisecond and the $V_1$ dependent term varies from about 0.47 volt per millisecond to about 0.15 volt per millisecond over the full range of input clock repetition rates assuming a maximum value of $V_1$ to be about 6 volt at the minimum clock frequency of interest. (Note that the value of $V_1$ used here is a measured one and is slightly less than the value predicted earlier from theoretical ramp slope considerations.)

The ratio of the time spent charging $C_1$ to the time spent discharging will be equal to the ratio of the discharge to the charge slope of $C_1$ (see waveform for $v_1$ drawn in Fig. 15b). If the charge slope (equal to the ramp slope) is much higher than the discharge slope the discharge time per input clock pulse will be approximately equal to the input clock pulse repetition period. Hence defining $T_c$ as the input clock repetition period we may determine $V_2$ more accurately as

$$V_2 \approx \frac{R_3}{R_2 + R_3} \left(V_1 + \frac{T_c k_d}{2}\right)$$

(7)

At this stage it is worth considering the flywheel type operation of the circuit. The output of the ramp circuit is attenuated by potentiometer R216 (Fig. 14) and is coupled to one input of the voltage comparator Q207. The output of the peak detector circuit is coupled to the other input of the comparator. If the input clock is interrupted, $v_2$ (by virtue of capacitor storage) will tend to remain unchanged. The ramp voltage will continue to rise until coincidence is reached at the comparator input. At this time a reset signal will be sent back to the ramp generator via the delay monostable Q201. Such reset signals constitute the inserted clock. Adjustment of R216 enables the ratio of the inserted clock repetition period to the input clock repetition period to be varied. These periods may be made very close if desired. In the present application the inserted clock repetition period is set about 15% higher than the incoming clock repetition period. If R216 is adjusted so that the ramp slope is too high, triggering of the voltage comparator will occur between input clock pulses and the circuit will tend to oscillate at high frequency. Increased comparator switching speed is provided by virtue of positive feedback via C206.

Define the following:

- $k_r$ is the ramp slope as seen at the output of the ramp generator.
- $k_1$ is a constant depending on the adjustment of potentiometer R216.
- $T_i$ is the period of the inserted clock.
If we neglect any DC unbalances we may put \( V_1 = k_r T_c \) for the time during which the input clock is applied. Assuming that \( V_2 \) does not have time to change while inserted clock pulses are generated we may write

\[
V_2 = k_1 k_r T_i
\]

and

\[
V_2 = \frac{R_s}{R_2 + R_3} \left( k_r - \frac{k_d}{2} \right) T_c
\]

Hence

\[
\frac{T_i}{T_c} = \frac{R_s}{k_1 (R_2 + R_3)} \left( 1 - \frac{k_d}{2k_r} \right)
\]

To satisfy the requirement that \( T_i \) be about 15% higher than \( T_c \) implies that \( k_1 \) have a value in the vicinity of 0·6. (Note that \( k_d/2k_r \) varies with \( T_c \) but has a maximum value of about 0·05 [at 640 hertz].)

The assumption that \( V_2 \) does not change during the time for which the input clock is omitted is not a very valid one when the input clock repetition frequency is low (640 hertz say) and the number of successive input clock pulses omitted is high (in this particular application 22 input clock pulses are omitted at the end of each record). Here the voltage \( V_2 \) will tend to rise with time while the input clock is omitted. Each successive ramp peak and each successive inserted clock repetition period will be higher than the previous one.

Some additional components to those already referred to have been used in the flywheel circuit. CR204 and CR205 are reference diodes having an extremely abrupt conduction characteristic. These diodes limit the comparator input to about \( \pm 5·7 \) volt. Normally these diodes are non-conducting and have no bearing on the circuit operation. CR202 together with CR203 (mentioned earlier) serve to limit the input voltage swing of the comparator. R214, R215 and R217 allow an adjustable DC offset to be added to the comparator ramp input. At high input clock frequencies (20·48 kilohertz maximum in this case) DC unbalances between the ramp output and the output of the peak charging circuit become very significant as the peak ramp voltage is low. Normally the system is adjusted by setting R216 to give the appropriate ratio of the incoming clock repetition period to the inserted clock repetition period at 640 hertz input clock frequency and then by adjusting R214 to give the same ratio at 20·48 kilohertz input clock frequency. Capacitive coupling of the inserted clock pulses is provided by C208. Such coupling is required to ensure that the inserted clock input E of the delay monostable Q201 cannot remain permanently in the low state. If direct coupling were used instead, a stable condition could exist for which the E input is low (ramp charged to maximum value) and the input clock A is inhibited from initiating pulses in the delay monostable.

In Fig. 16 oscilloscope traces of the ramp output in relation to the input clock are shown for basic input clock frequencies in the range 640 hertz to 20·48 kilohertz. For these traces a record consisting of three words (providing 18 clock pulses and an EOW gap equivalent to two missing clock pulses) and an EOR gap (of one word plus an EOW gap in duration) has been used. In all cases two excursions of the ramp output occur during an EOW gap and from 18 to 19 excursions occur during an EOR gap (22 missing input clock pulses). During the EOR gap the ramp period progressively increases up to 1·20 times its initial value for an input clock frequency of 640 hertz. Ramp period changes throughout the EOR gap become progressively less at higher input clock frequencies.

In Fig. 17a oscilloscope traces for voltages \( v_1 \) and \( v_2 \) in the charging circuit are shown in relation to the input clock for 640 hertz frequency only. At this frequency, changes in \( v_2 \) over a record are a maximum (for the frequency range of interest).

Oscilloscope traces showing the relationship between the input clock A, the inserted clock E and the output clock D (an effective summation of the other two clocks) are reproduced in Fig. 17b.

When input clock pulses are omitted indefinitely the circuit will normally oscillate at a low frequency (285 hertz approximately for the particular circuit used). The free-running period is related to the limiting value of \( V_2 \) set by CR204 and CR205, the slope of the ramp input to comparator Q207 (i.e. depends on \( k_1 \)) and the extent of ramp non-linearity at high output voltages (which in this circuit is quite significant).

There is also a stable condition for which the circuit will not oscillate. This will occur when the ramp circuit has charged to a maximum value and no inserted clock pulses are gen-
crated. If the circuit is triggered by even a single clock pulse or noise pulse oscillations will
commence.

Another requirement of the electronic flywheel is that it generate a "deskewed" clock
which we will define as a clock signal (applied to a number of parallel digital data lines) which
enables all data lines corresponding to each byte of data to be interrogated at a time when
all data lines have had time to change and at a time prior to the arrival of the next byte of data.
In this particular application the parallel lines to be interrogated are associated with an appro-
priate digital register (to be discussed in Sec. 4.3.4).

For data recorded serially only one level change will be generated per data bit (excluding
parity errors). Hence a deskewed clock which occurs a fixed time duration (which would need
to be somewhat less than the minimum repetition period of interest [48.8 microsecond] to
enable data reproduced at all speeds to be catered for without switching) after each input clock
pulse would be sufficient in that case. However, as will be indicated shortly, the generation of a
deskewed clock which is delayed with respect to the input clock by a time interval proportional
to the input clock repetition period, increases immunity from noise.

For data recorded in parallel however the input clock pulse generator (Sec. 4.3.1) may
produce a number of input clock pulses per byte of data. Dynamic skew characteristics of the
reproduced data will define the time difference between the various input clock pulses generated
for each byte of data. To read such data over the full range of tape speeds, a clock delayed by
a time inversely proportional to tape speed is required since time differences arising due to
dynamic skew will be very nearly inversely proportional to tape speed.

The use of a second comparator as indicated in Figs. 13 and 14 enables the required deskewed
clock to be generated. In this instance the ramp output is coupled to one side of the comparator
Q208 via potentiometer R220. A specified fraction of the charging circuit output voltage $V_2$
as set by R212 and R213 is coupled to the other comparator input. R218 allows for DC adjust-
ment similar to that required for the inserted clock comparator Q207. Increased switching speed
of the comparator is provided by positive feedback via C207.

In the present application the comparator has been set to switch about 40% of an input
clock pulse repetition period after the arrival of the previous input or inserted clock pulse. At
such a time the digital data register would have had adequate time to settle.

By coupling the deskewed clock output F (Figs. 13 and 14) back into the delay monostable
Q201 only one clock pulse per data bit for the serial system or per data byte for the parallel
system is guaranteed. Whenever the F input is low the monostable will not respond to pulses
either on the A input (input clock) or the E input (inserted clock). For the first nominal 40%
of the input repetition period the F input will be low. Hence a certain level of immunity to
noise is achieved. It may be assumed that the G input to the NAND gate providing coupling
between the comparator and the delay monostable is high whenever input clock pulses are being
received.

In Fig. 18a an oscilloscope trace of the deskewed clock indicating its relation to the input
clock in the vicinity of the EOW gap is shown. It is to be noted that the negative going transitions
are coincident with the input clock and the positive going transitions (constituting the deskewed
or delayed clock) occur about 40% of an input clock repetition period after the arrival of each
input clock pulse. At the time of arrival of the first input clock pulse after an EOW gap the
deskewed clock is always high and hence the first input clock pulse will trigger the delay monostable.

If the deskewed clock were generated normally throughout an EOR gap (during which
a large number of inserted clock pulses are generated) there would be no guarantee that the
deskewed clock output F would be high at the time of arrival of the first input clock pulse after
the EOR gap and hence the output clock D may not immediately synchronize with the input clock
as required. To prevent such an occurrence an inhibit signal G, which switches from a normally
high state to a low state after 9 successive inserted clock pulses have been counted, and remains
in that state until the arrival of the next input clock pulse, is provided by the control signal
generator discussed in Sec. 4.3.3. In Fig. 18b an oscilloscope trace of the deskewed clock is
shown in conjunction with the input clock in the vicinity of the EOR gap. The relatively long
period during which the deskewed clock is high corresponds to the time during which the EOR
gap inhibit signal G is low. The filter circuit comprising R223 and C209 delays the application
of inhibit signals for the delay monostable long enough to ensure that the first input clock
pulse A, after an EOR gap, is not inhibited by the deskewed clock signal F.
One of the most important requirements of the electronic flywheel is that only one stable condition (corresponding to one output clock pulse per input clock pulse except during gaps) be possible when an input clock is applied. Certain other stable conditions are possible if some of the operating characteristics are incorrectly adjusted. A characteristic of particular importance is the ratio of the free-running period to the input clock period (adjusted via R216). If the free-running period is set too close to the input clock period “double” frequency operation may occur in which an inserted clock pulse is generated between each successive pair of input clock pulses. Hence in that case two ramp peaks would be generated between each pair of input clock pulses and the output $V_t$ of the charging circuit would remain low. For the circuit of Fig. 14 adjusted as described earlier double frequency operation does not occur. Another stable operating mode is possible in which the output of the peak charging circuit charges to a voltage higher than that for normal operation. Under these conditions output clock pulses would not be generated for each input clock pulse. This mode of operation is very likely if the deskewed clock is delayed later than the mid-time between input clock pulses. It is also favoured by data containing gaps which represent a fairly large proportion of the total time especially if relatively long time constants are used in the peak charging circuit. In the application under discussion it has been found that for records composed of more than two words between EOR gaps this latter operating mode does not arise. It is to be noted that in all cases correct operation represents at least one of the possible operating modes.

Because the voltage drops across the capacitors in the peak charging circuit can only change relatively slowly the flywheel will not respond instantaneously to the application of an input clock but will take some time to change from the free-running mode to synchronized operation. However, since analogue tape transports will also not respond instantaneously on switch on, the small additional delays were not considered to be significant. It has been found that the time to change from the free-running mode to synchronized operation at 20-48 kilohertz input clock frequency is less than one second. Similarly the time to change from synchronized operation at 20·48 kilohertz to synchronized operation at 640 hertz is also less than one second. If instantaneous operation were required it would be necessary to initially break the flywheel circuit at Point $x$ (Fig. 14) and apply a suitable DC potential to the comparator side. With such an arrangement the free-running frequency of the system could be adjusted just below the required value of input clock frequency. However since the flywheel may not free run when switched on the application of an input pulse may be required to start oscillations.

The flywheel circuit of Fig. 14 is required in both the serial and the parallel systems of recording. For the serial system, inserted clock pulses generated during the EOW and EOR gaps may be counted (Sec. 4.3.3) and used to synchronize the data. In addition clock pulses are inserted if input pulses are missed due to tape dropouts or for other causes. For the parallel system gaps are not introduced but clock pulses are inserted if input pulses are missed as in the serial system. A deskewed clock generated by the flywheel enables data recorded either serially or in parallel to be read at suitable times. Further the deskewed clock is used to provide a measure of immunity to noise in association with the incoming clock. All the above functions are automatically performed without the need for switching any components in the flywheel circuit over the required input clock frequency range of 640 hertz to 20·48 kilohertz. One particular advantage of the flywheel circuit used is that ramp linearity is not of prime importance since the peak charging circuit follows any non-linearity.

The flywheel circuit which has been described has a much wider field of applications than described here. Whereas the input clock frequency range of interest here is only 640 hertz to 20·48 kilohertz the flywheel circuit as indicated in Fig. 14 performs satisfactorily over the range 300 hertz to 30 kilohertz (100 to 1 frequency ratio). In any application where “missing” clock pulses must be inserted the flywheel circuit is ideally suited. The repetition period of the inserted clock may be set very close to that for the input clock (the flywheel inserted clock has been operated within 5% of the input clock) but care must be exercised to avoid “double” frequency operation.

4.3.3. Control Signal Generator

The control signal generator (indicated in the block schema of Fig. 7) is required to generate:

(i) An inhibit signal G during the EOR gap for use with the electronic flywheel in the case of data recorded serially only.
(ii) Appropriate inhibit and clock signals for the serial to parallel converter (Sec. 4.3.4) and associated parity check circuits.

(iii) Word read command and frame synchronizing signals for use with a digital computer.

(iv) Clock signals to enable the digital data to be read into data stores used in conjunction with displays (Secs. 4.3.5 and 4.3.6).

(v) A clock signal for use with the tape machine preset stop signal generator (Sec. 4.3.7).

The block schema of Fig. 19 indicates in general terms the operating principle of the control signal generators for both the serial and the parallel systems. For simplicity not all the control functions have been indicated. For every 20 flywheel output clock pulses received by the bit counter in the serial system an output pulse is generated (each word has 20 bit durations associated with it), and for every 4 flywheel output clock pulses received by the byte counter in the parallel system an output pulse is generated (each word has 4 byte durations associated with it). Similarly the word counter counts the bit (or byte) counter output pulses (one for each word) but in this case the maximum count registered will be dependent on the number of words recorded per frame.

Synchronization of the bit (or byte) and the word counters is provided by the word and frame synchronizing signals generator. For the serial system counting of consecutive inserted flywheel clock pulses, which are received in the absence of flywheel input clock pulses, is employed in the synchronizing signals generator, whereas for the parallel system the recorded information is examined by the synchronizing signals generator.

The bit (or byte) counter outputs and the word counter outputs are decoded respectively by the serial to parallel converter control signal generator and the display control signal generator.

As the requirements of the control signal generators used respectively for the serial and parallel systems of digital recording are different the generators will now be considered separately.

A logic diagram of the control signal generator for the serial system is drawn in Fig. 20. Further subdivision of the generator in relation to the various functions performed is indicated by blocks within dotted lines in the above figure. The timing relationship of some of the relevant signals generated is shown in Fig. 21.

Generation of appropriate control signals is made convenient by the use of bit and word counters. For each word 20 output clock pulses D are generated where 2 of these correspond to inserted clock pulses. To provide a divide-by-20 circuit the bit counter uses a decade counter Q305 followed by a count-by-2 flip flop Q307A. Records containing up to 100 words are accommodated using two decade counters Q309 and Q313 in the word counter.

Reset signals are required to synchronize the bit and the word counters. To generate these, inserted clock pulses E are counted using a decade counter Q304, which is reset whenever a clock pulse A (Fig. 8) is generated. Decoding of this counter to provide separate outputs when 2 and when 9 consecutive inserted clock pulses are counted is performed using a BCD to decimal decoder Q308. The decoded 9 output presets a flip flop Q307B which is cleared by input clock pulses A. The Q output of this flip flop resets the word counter to the zero count state whereas the Q̅ output (which is normally high but which reverts to the low state during the EOR gap) is coupled back to NAND gate Q301A to prevent the entry of clock pulses D into the bit counter when this output is low. The Q̅ output of flip flop Q307B constitutes the EOR inhibit signal G which is taken to the electronic flywheel and also the frame synchronizing signal N required for the digital computer.

Ideally the EOR reset signal (used for resetting the word counter) is also sufficient for synchronizing the bit counter. However if records are long, the missing of an output clock pulse (due for instance to a tape dropout having a duration of more than 2 input clock repetition periods) would cause misalignment of the remainder of the data in that record. For this reason additional reset signals (which normally only check that the bit counter is synchronized) are generated during the EOW gaps. The bit counter is decoded to provide an inhibit signal at the output of inverter Q303D which only allows the generation of reset signals near the end of each word (within the last four count states). This reduces the likelihood of the bit counter being reset if, due to tape dropout or other cause, two successive inserted clock pulses are generated at some time other than during an EOW gap.

To avoid any ambiguity in relation to clocking and resetting of the bit and the word counters the reset signals have been arranged to occur at different times to the clock signals for these
counters. In effect, resetting of the counters occurs in synchronism with the leading edges of the output clock pulses D. Conversely clocking of the counters occurs in synchronism with the trailing edges of the output clock pulses D. By resetting the bit counter to a count state of 19 the first D pulse after an EOW gap sets this counter to the zero count state.

To indicate timing, each word will be broken up into time intervals associated with each bit. Define $B_r$ as a quantity which takes on a high (logical “one”) value for the period during which the bit counter registers a count of $r$. Note $0 \leq r \leq 19$ for the bit counter. Time intervals associated with $B_6$ to $B_{18}$ will be equal to the input clock A repetition period, those associated with $B_7$ and $B_{16}$ will be higher since the repetition period of the inserted pulses is higher, and that associated with $B_{19}$ will be smaller (refer to lower trace of Fig. 17b and also to Fig. 21). Using the above logic notation we may express the following decoded outputs of the bit counter thus:

$$U = (B_{18} + B_{17} + B_{18} + B_{19})'$$

where $U$ is the output of inverter Q303D and is taken to the analogue machine preset stop signal generator. (Note that the dash is the “inverting” notation.)

$$I = B_{18}$$

where $I$ is the output of NOR gate Q306C and constitutes the word read command signal for the digital computer.

Filter components R302 and C302 prevent the generation of additional very short duration pulses on the $I$ output as a result of propagation delays in the bit counter and associated logic devices. The read command signal $I$ has a minimum duration of about 50 microsecond at the maximum data rate used.

Positive going transitions of the deskewed clock $F$ occur about 40% of an input clock repetition period (Sec. 4.3.2) after the leading edges of the output clock pulses $D$. After two inversions (through Q303E and Q303A) the $F$ signal is AC coupled to NAND gate Q301B. In this way short duration (approximately 300 nanosecond) positive pulses designated by $F_1$ are generated. The output $M$ of NAND gate Q301B is a series of negative short duration pulses (Fig. 21) inhibited for the period associated with $B_{16}$ to $B_{19}$. Logically we may write:

$$M = [(B_{18} + B_{17} + B_{18} + B_{19})'F_1]$$

where $K$ is a control signal returned from the serial to parallel converter.

The output $H$ of NAND gate Q301A is given by

$$H = (DG)' = D' + G'$$

and the output $J$ of NOR gate Q306A is not readily definable symbolically but is as indicated in Fig. 21.

As indicated in Fig. 20 control signals $H$, $J$, $K$, $L$ and $M$ are connected to the serial to parallel converter.

Words will be represented using a similar notation $W_n$ to that used for bits. In the absence of reset signals the word counter will count up to 99. For records of less than 99 words in length (excluding the EOR gap) resetting to the zero count state (associated with $W_0$) will occur during an EOR gap. Hence the first information word in a record is $W_1$.

Front panel mounted decimal thumbwheel switches S301 and S302 in association with BCD to decimal decoders Q310 and Q313 allow any word between 1 and 99 to be selected for display (Sec. 4.3.6). For instance in the arrangement shown in Fig. 20 a high output on NOR gate Q311B will occur only at $W_{16}$ where 16 is the number set on the thumbwheel switches. For generality let $W_n$ represent the selected word. For the selected word an output $I_n$ will be generated where

$$I_n = (IW_n)' = (B_{18}W_n)'$$
Thus \( I_n \) is a control signal which is normally in the high state but which switches to the low state at \( B_{18} \) of \( W_n \). \( I_n \) is used in conjunction with data displays (Sec. 4.3.6).

Displays of the fixed and the time-of-day data (Sec. 2) are also required. All such data are contained in one specific word per record which we will assume is \( W_1 \). Control signals \( I_{11} \) and \( I_{12} \) are required for use with these displays and associated circuits where

\[
I_{11} = [(I W_1)' + F]'
= F' W_1
= F' B_{18} W_1
\]

and

\[
I_{12} = [(I W_1)' + F']'
= F B_{18} W_1
\]

Hence \( I_{11} \) and \( I_{12} \) are signals which are normally low but which take on a high value during \( B_{18} \) of \( W_1 \). \( I_{11} \) is high during the earlier part of \( B_{18} W_1 \) corresponding to \( F \) low and \( I_{12} \) is high during the latter part of \( B_{18} W_1 \) corresponding to \( F \) high.

A logic diagram of the control signal generator for the parallel system is drawn in Fig. 22. Further subdivision of the generator in relation to the various functions performed is indicated by blocks within dotted lines in the above figure. The timing relationship of some of the relevant signals generated is shown in Fig. 23.

As mentioned in Sec. 2 the end of a word and the end of a record are indicated by information recorded digitally on two tracks (tracks 5 and 6). Four bytes of data are recorded per word. The data is recorded on tracks 1 to 4 and lateral parity is recorded on track 7. The second of two consecutive recorded “ones” on track 5 indicates the presence of the last of the four bytes in the word and the fourth of four consecutive recorded “ones” on track 6 indicates the presence of the last byte in the record.

Generation of appropriate control signals is made convenient by the use of byte and word counters. For each word, 4 output clock pulses \( D \) (Sec. 4.3.2) are generated. A divide-by-four counter made up of flip flops Q359A and Q359B is used as the byte counter. Records containing up to 100 words are accommodated using two decade counters Q362 and Q363 in the word counter.

Appropriate signals are generated to reset the byte and the word counters. Since synchronising information is contained in the digital data recorded on tracks 5 and 6 it is essential that this data be first read. Digital outputs \( e_5 \) and \( e_6 \), which change state according to the recorded data on tracks 5 and 6, are derived from the serial to parallel converter (Sec. 4.3.4). Serial to parallel conversion of the data recorded in parallel is used to convert the 4 serial bytes into one 16-bit parallel word with an additional parity checkbit. Any changes in state of \( e_5 \) and \( e_6 \) occur during the time that \( A_5 \) and \( A_6 \) inputs (Fig. 9) respectively are applied to the serial to parallel converter.

Short duration positive going pulses starting at the trailing edges of the \( D \) pulses are generated using AC coupling in conjunction with NAND gates Q357A and Q357B, which are connected as inverters. These pulses clear flip flop Q356A when \( e_5 \) is low and clear flip flops Q356B, Q358B and Q358A when \( e_6 \) is low. Short duration positive pulses \( S \) starting at the positive going transistors of the deskewed clock \( F \) are also generated in a similar manner. These pulses clock flip flops Q356A and Q356B (\( JK \) flip flops with \( J = 1 \) and \( K = 1 \)) when \( e_5 \) and \( e_6 \) are high respectively. After two consecutive “ones” are read on track 5 the \( Q \) output of flip flop Q356A will undergo a positive transition at the time the deskewed clock \( F \) goes high. This latter transition is AC coupled to NAND gate Q357C which is gated also by the \( S \) clock. Hence an output (negative going) pulse will be generated by Q357C in synchronism with \( S \) whenever
2 consecutive “ones” are reproduced on channel 5. This latter output checks that the byte counter is in the count-of-3 state. When the byte counter receives the next clock pulse D it reverts to the count-of-0 state which corresponds to the first byte in the word. Whenever 4 consecutive “ones” are read on track 6 the Q output of flip flop Q358B will switch high in synchronism with the S clock. This latter output presets flip flop Q358A via NAND gate Q357D in synchronism with the S clock. A reset pulse N coincident with the D output clock pulse is generated by NOR gate Q360A and resets the word counter to the zero state when the D pulse following the last “one” read from track 6 arrives. Hence the first word in a record will be $W_0$ (using the same notation as used earlier for the serial system). The reset pulse N constitutes the frame synchronizing signal required for the digital computer.

For records less than 100 words in length the generation of word counter reset pulses is essential to maintain synchronism whereas the generation of byte counter reset pulses is not normally required to maintain synchronism. Usually the byte counter reset pulses merely check that the state of the byte counter is correct.

Suitable clock signals (Fig. 23) for use with the serial to parallel converter are generated using four NOR gates Q353, four NAND gates Q352 and four inverters forming part of Q351 in conjunction with the byte counter outputs and the S signal. These clock pulses are short duration positive pulses in time synchronism with the S signal. $X_1$ occurs only in association with the first byte, $X_2$ occurs only in association with the second byte and so on. Other signals required by the serial to parallel converter are the S signal described earlier and a signal designated $U_1$ which is normally low but which reverts to the high state for the duration of the first byte (i.e. for the time the byte counter is in the count-of-0 state).

A pulse starting at the trailing edge (negative going transition) of the $X_t$ pulse clears the Q output of flip flop Q361 (i.e. switches to low state) which is preset back to the high state in synchronism with the next D pulse. The Q output of flip flop Q361 constitutes the read command signal I required for the digital computer. The read command signal I is generated for each word and has a minimum duration of about 145 microsecond (corresponding to the maximum data rate of 1024 words per second).

Data display requirements are identical to those for the serial system. Front panel mounted switches S301 and S302 in association with BCD to decimal decoders Q364 and Q365 allow any word between 0 and 99 to be selected for the display of “sampled” data (Sec. 4.3.6). A control signal $I_n$ (Fig. 23) having the same time relationship as the I signal except that it is only generated for the selected word is made available for use with the sampled data display. Similarly control signals $I_{11}$ and $I_{12}$ (Fig. 23) are generated for use with the fixed data and time-of-day displays. Both are generated in association with $W_1$; $I_{11}$ is in time synchronism with $X_1$ and $I_{12}$ is in time synchronism with I. Note that word $W_0$ for the parallel system may be used for data recording since it is not required for the purpose of synchronization.

4.3.4. Serial to Parallel Converter

Re-arrangement of the digital data as read from the tape machine is required for ease of handling by a digital computer. (Many digital computers will accept a 16-bit parallel input.) For data recorded serially a 16-bit serial to a 16-bit parallel conversion is required whereas for data recorded in parallel a 4-byte serial (4 data bits per byte) to a 16-bit parallel conversion is required. In addition the generation of overall parity checkbits for each word is required. As the requirements for the serial to parallel converters used respectively for the serial and the parallel systems of recording are different the converters will be considered separately.

A logic diagram of the serial to parallel converter used for the serial system is drawn in Fig. 24. Parity checking logic is also indicated in this figure.

For ease of explanation define $b_0$ to $b_{17}$ as the digital information (either a “one” or a “zero”) recorded sequentially, starting at $b_{10}$ for each data word. Note that $b_{18}$ and $b_{19}$ are not
included because EOW gaps (2 bit durations) are used. The following table summarizes the recording format used.

<table>
<thead>
<tr>
<th>Bit Location</th>
<th>B19</th>
<th>B0</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>B4</th>
<th>B5</th>
<th>B6</th>
<th>B7</th>
<th>B8</th>
<th>B9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Information recorded on Data Track</td>
<td>—</td>
<td>$b_0$</td>
<td>$b_1$</td>
<td>$b_2$</td>
<td>$b_3$</td>
<td>$b_4$</td>
<td>$b_5$</td>
<td>$b_6$</td>
<td>$b_7$</td>
<td>$b_8$</td>
<td>$b_9$</td>
</tr>
<tr>
<td>Information recorded on Parity Track</td>
<td>—</td>
<td>$b_0'$</td>
<td>$b_1'$</td>
<td>$b_2'$</td>
<td>$b_3'$</td>
<td>$b_4'$</td>
<td>$b_5'$</td>
<td>$b_6'$</td>
<td>$b_7'$</td>
<td>$b_8$</td>
<td>$b_9$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Location</th>
<th>B10</th>
<th>B11</th>
<th>B12</th>
<th>B13</th>
<th>B14</th>
<th>B15</th>
<th>B16</th>
<th>B17</th>
<th>B18</th>
<th>B19</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Information recorded on Data Track</td>
<td>$b_{10}$</td>
<td>$b_{11}$</td>
<td>$b_{12}$</td>
<td>$b_{13}$</td>
<td>$b_{14}$</td>
<td>0</td>
<td>$p$</td>
<td>—</td>
<td>—</td>
<td>$b_0$</td>
<td></td>
</tr>
<tr>
<td>Information recorded on Parity Track</td>
<td>$b_{10}'$</td>
<td>$b_{11}'$</td>
<td>$b_{12}'$</td>
<td>$b_{13}'$</td>
<td>$b_{14}'$</td>
<td>$b_{15}'$</td>
<td>1</td>
<td>$p'$</td>
<td>—</td>
<td>—</td>
<td>$b_0'$</td>
</tr>
</tbody>
</table>

B0 to B19 refer to bit locations within the time allocation for the recording of a word. At B17 an even longitudinal parity character $p$ is recorded such that

\[
p = 1 \text{ if } \sum_{r=0}^{15} b_r \text{ is odd}
\]

and

\[
p = 0 \text{ if } \sum_{r=0}^{15} b_r \text{ is even.}
\]

At B16 a dummy character $b_{36} = 0$ is recorded to enable odd lateral and even longitudinal parity conditions to be satisfied at B17.

Temporary storage (for the time allocated per bit) of digital data recorded on the data and the parity tracks is provided respectively by flip flops Q404A and Q404B. Each time a “one” is read from the data track, input $A_1$ will switch from its normally high state to the low state for approximately 4 microsecond (Sec. 4.3.1) and each time a “one” is read from the parity track $A_2$ will switch in a similar manner. The $A_1$ and the $A_2$ inputs preset the respective Q outputs of flip flops Q404A and Q404B to the “one” state whenever these inputs switch to the low state (i.e. whenever “ones” are read). The $H$ input derived from the control signal generator (Fig. 20) consists of a series of positive pulses (of 1-4 microsecond duration approximately) in time synchronism with the flywheel output clock signal $D$. During part of the EOR gaps (when $G$ [Fig. 21] is low) the $H$ output remains high.

\[
H = D' + G'
\]

(Sec. 4.3.3)

Clear signals ($A_1H'$ and ($A_2H'$) are taken respectively to flip flops Q404A and Q404B. Since the $A_1$ or $A_2$ pulses are always longer in duration that the $D$ pulses and since the leading edges of the $A_1$ or $A_2$ pulses and the $D$ pulses are nominally coincident (but more precisely the $D$ pulses are slightly delayed with respect to the $A_1$ or $A_2$ pulses which effectively initiate them) clear pulses (low level) will be generated only when a “zero” is read (i.e. when a “one” is read on the other track). In Fig. 25 oscilloscope traces indicate the time relationship between $A_1$, $A_2$, $H$ and clear signals for flip flops Q404A and Q404B. Changes in state of these flip flops always occur in synchronism with the leading edges of the $D$ (or $H$) clock.

Serial to parallel conversion of the digital data is performed using four 4-bit shift registers Q406 to Q409 connected as a 16-bit shift register. The output of the data flip flop Q404A is connected to the serial input of the Q406 shift register. Clocking of the shift register is performed by the $M'$ signal where $M$ is a signal (Fig. 21) generated in the control signal generator. $M'$ is normally low but switches high for a short period (approximately 300 nanosecond) starting at the time the deskewed clock goes high. Shift register clock pulses are generated only in associ-
ation with bits $b_0$ to $b_{15}$. Whenever a clock pulse is applied to the shift register the level on the serial input is transferred to the first output and all the other outputs shift one place to the "right." Hence on the application of the sixteenth clock pulse (transfer of data occurs on the negative transition of the clock) the 16-bit register will contain the data word with $b_{15}$ being the last bit entered into the register (Fig. 24). Since the shift register does not receive another clock pulse until $b_0$ of the next word is read the contents of the register will remain unchanged from $B_{18}$ to $B_{19}$ (refer to Sec. 4.3.3 for definition). The outputs of the shift register have been designated $b_0$ to $b_{15}$ but it must be remembered that these outputs are a true representation of the digital data only over part of a word repetition period.

Whenever a clock pulse is applied to the shift register (i.e. for $b_0$ to $b_{15}$) the lateral parity of the information as read by flip flops Q404A and Q404B is checked using the exclusive OR circuit Q405A and NAND gate Q402C. If the parity is even (two "ones" or two "zeros") a negative going preset pulse will be transferred to flip flop Q403B. At the beginning of each word the Q output of flip flop Q403B is cleared to the low state (i.e. on the positive excursions of the J control signal [Fig. 21] which occur at the start of each word). Hence if one or more lateral parity errors are detected in a word the Q output of flip flop Q403B, designated as $p_1$, will switch to a high state which will be maintained until the start of the next word.

The longitudinal parity of the word as read from the data track is checked using the circuit indicated in Fig. 24. At the beginning of each word the Q output of flip flop Q403A is cleared to the low state. This latter flip flop ($J$-$K$ flip flop with $J = K = 1$) toggles each time a clock pulse is applied. A signal $L'$ is connected to the clock input where

$$L = (B_{18} + B_{19})KF_1$$  

(4.3.3)

As indicated earlier $F_1$ represents a signal which is normally low but which switches high for a short time (300 nanosecond approximately) whenever the deskewed clock $F$ (Fig. 21) switches from the low to the high state. $K$ is the Q output of data flip flop Q404A. As can be seen from the above equation the clock $L'$ will remain high for the time interval associated with $B_{18}$ and $B_{19}$ and hence flip flop Q403A will not change state in this time. Otherwise clock pulses will be generated for every "one" read on the data track. If the parity is correct an even number of clock pulses will be generated and the Q output of flip flop Q403A, designated as $p_2$, will be low after $b_{15}$ has been read. Conversely if the even longitudinal parity condition is not satisfied output $p_2$ will be high after $b_{15}$ has been read.

An overall parity check character $p$ (where $p = p_1 + p_2$) is also generated. When an error is detected on either or both of the lateral and the longitudinal check circuits $p$ will switch to the high state.

The parallel output comprising the 16 data bits ($b_0$ to $b_{15}$) and one or two parity bits ($p$ or $[p_1$ and $p_2$]) is taken to a digital computer and also to the data store (Sec. 4.3.5) associated with the data displays. Reading of the parallel output is performed within the time associated with $B_{18}$ (see waveforms relating to $I$, $I_n$, $I_1$, and $I_{12}$ in Fig. 21). During this time of reading, the data is correctly arranged in the output register and no data changes are possible.

For the parallel system of recording a serial to parallel converter having the logic arrangement depicted in Fig. 26 is used. Each time a "one" is read from a particular track the associated data output ($A_1$ to $A_7$ [Fig. 9] corresponding to tracks 1 to 7) will switch from a normally high state to a low state for approximately 4 microsecond thus presetting the Q output of the associated temporary storage flip flop (Q450A to Q453A) to the high state. Each time a flywheel output clock pulse $D$ arrives it sets the associated Q output of the above flip flop to the high state. Hence in the absence of a pulse (i.e. when a zero is read) on any given preset input the Q output will be set to the low state. NAND gates Q455A and Q455B which are connected as inverters merely provide buffering for the $D$ input which would otherwise be loaded excessively (taking into consideration loading elsewhere).

The Q outputs of temporary storage flip flops Q450A to Q453A have been labelled $e_1$ to $e_5$, $e_6$, and $e_7$ are returned to the control signal generator (Sec. 4.3.3 and Fig. 22) and are used for synchronizing the byte and the word counters, $e_1$ to $e_4$ are connected to four separately clocked 4-bit bistable latches Q456 to Q459. Whenever the clock signal for a 4-bit latch switches to the high state the input data (on $1D$ to $4D$) is transferred to the output ($1Q$ to $4Q$) where it is retained after the clock switches back to the low state. Clock signals $X_1$ to $X_4$ are short duration positive pulses starting in time synchronism with the positive transitions of the deskewed clock. $X_1$ occurs only in association with the first byte, $X_2$ occurs only in association with the second byte

$$X_1 = \overline{\overline{X_1}}$$

$$X_2 = \overline{\overline{X_1}}$$

$$X_3 = \overline{\overline{X_1}}$$

$$X_4 = \overline{\overline{X_1}}$$
and so on. Hence between the time the $X_4$ clock pulse is applied and the time the $X_1$ clock pulse for the next word is applied the parallel output $b_0$ to $b_{16}$ from the 4-bit latches holds digital information corresponding to the last word read.

Data outputs $e_1$ to $e_7$ are connected to the parity checker Q454 to enable lateral parity to be checked. If the parity is odd the output of the parity checker will be low (normal); if the parity is even the output will be high (indicating an error). Interrogation of the output of the parity checker is performed using the $S$ control signal (where $S = X_1 + X_2 + X_3 + X_4$) in conjunction with NAND gate Q455D. If a parity error is detected in one or more bytes of data corresponding to a particular word then the Q output $p_1$ of flip flop Q453B will be preset to the high state. At the beginning of each word (i.e. on the positive going transitions of $U_1$ [Fig. 23]) $p_1$ is cleared to the low state. $U_1$ is AC coupled via NAND gate Q455C to the clear input of flip flop Q453B so that the clear pulse is of relatively short duration (300 nanosecond approximately). Hence between the time the $X_4$ clock pulse is applied (to 4-bit latch Q459) and the time the $X_1$ clock pulse for the next word is applied (to 4-bit latch Q456) the parity output $p_1$ indicates whether any parity errors have been detected in the last word read.

The parallel output comprising 16 data bits ($b_0$ to $b_{15}$) and the parity bit $p_1$ are taken to a digital computer and also to the data store (Sec. 4.3.5) associated with the data displays. Reading of the parallel output is performed within the time associated with $I$ (Fig. 23) which constitutes a read pulse for each word. Similarly a read pulse $I_n$ (Fig. 23), having the same time relationship in the word repetition period as $I$, is generated for use with the sampled data display. $I_{11}$ and $I_{12}$ (where $I_{11} + I_{12} = I_n$ putting $n = 1$ in $I_n$ [Fig. 23]) are generated for use with the fixed data and time-of-day displays.

The parity checking arrangement employed for both the serial and the parallel systems provides an indication of whether there is an error (or a likely error) in a word. In the case of the serial data for which lateral and longitudinal parity bits are recorded it would be possible to locate single errors in a word and correct for these. However, considerable increase in circuit complexity would result. Since an occasional error is of no consequence for the type of data recording envisaged (provided that the word in error can be located and ignored) the generation of overall word errors is considered adequate. Such error information may be used by a digital computer which may be programmed to ignore any word for which an error is indicated or to suitably label any output data which uses information contained in such a word.

4.3.5. Data Store

To facilitate identification of magnetic tape records and to assist in locating any specific regions of interest on a particular tape the following are displayed by the digital interface.

(i) Fixed Data

Includes (a) Run number composed of four decimal digits where each digit is recorded in 1-2-4-8 binary coded decimal (BCD).

(b) Month-of-the-year (1 to 12) and day-of-the-month (1 to 31) information recorded in 1-2-4-8 BCD using a total of 11 bits (5 for month-of-the-year and 6 for day-of-the-month).

(ii) Time of Day

Recorded as hours (0 to 23), minutes (0 to 59) and seconds (0 to 59) in 1-2-4-8 BCD using a total of 20 bits (6 for hours, 7 for minutes and 7 for seconds).

As indicated in Sec. 2 one data word ($W_i$) per frame (or record) is allocated for the recording of the fixed data and time-of-day information. Four such words (which we will define as $W_{11}$, $W_{21}$, $W_{31}$ and $W_{41}$) recorded in successive records specify one complete reading of the above data. A two bit identifier ($b_0$ and $b_1$) at the beginning of each $W_i$ word identifies the information in that word.

In order to display the appropriate data using suitable numeric indicators it is essential that the data be read and stored. A logic diagram of the fixed data and time-of-day store is given in Fig. 27. Digital outputs $b_0$ to $b_{16}$ from the serial to parallel converter (either for the serial system [Fig. 24] or for the parallel system [Fig. 26]) are coupled into the store as indicated. The data are stored using 4-bit bistable latches Q505 to Q517A where storage allocation is as follows:

(i) 14 bits corresponding to $W_{11}$ for minutes and seconds.

(ii) 12 bits corresponding to $W_{21}$ for hours and day-of-the-month.
(iii) 9 bits corresponding to $W_{31}$ for month-of-the-year and the first digit of the run number.

(iv) 12 bits corresponding to $W_{41}$ for the remaining three digits of the run number.

Clocking (during which time the logic levels on the D inputs of the bistable latches are transferred to the Q outputs) for store sub-sections (i) to (iv), is provided by signals designated $Y_1$, $Y_2$, $Y_3$ and $Y_4$ corresponding respectively to $W_{11}$, $W_{21}$, $W_{31}$ and $W_{41}$. Decoding of the identifier $b_0b_1$ according to the table below is required before an appropriate clock pulse ($Y_1$ to $Y_4$) is generated.

<table>
<thead>
<tr>
<th>Word Identifier</th>
<th>$W_{11}$</th>
<th>$W_{21}$</th>
<th>$W_{31}$</th>
<th>$W_{41}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$b_0$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$b_1$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

On the positive going transition of the control signal $I_{11}$ (Figs. 20, 21, 22 and 23) digital data $b_0$ and $b_1$ is entered into store Q505A (Fig. 27). Using NOR gates Q504 the output of the above store is decoded to provide a high level output successively on each gate (with low outputs on the other three) according to the $b_0b_1$ input. Using the outputs of the NOR gates in conjunction with the NAND gates Q503, the control signal $I_{12}$ which always occurs after $I_{11}$ as indicated in Figs. 21 and 23) is effectively coupled to the appropriate store sub-section where

$Y_1 = W_{11} I_{12}$

$Y_2 = W_{21} I_{12}$

$Y_3 = W_{31} I_{12}$

$Y_4 = W_{41} I_{12}$

NAND buffers Q501 and Q502 have adequate “fan out” capability to meet the requirements of the store clocks ($Y_1$ to $Y_4$).

The store outputs have been designated as 1Q to 4Q and where required elsewhere the 1Q to 4Q outputs have also been indicated (complementary outputs also available from the 4-bit bistable latches used).

Display of any word as selected by front panel decimal thumbwheel switches S301 and S302 (Figs. 20 and 22) is also required using suitable numeric indicators. Lamps are required to indicate the detection of an error by either or both of the lateral and the longitudinal parity check circuits for data recorded serially or by the lateral parity check circuit for data recorded in parallel (no longitudinal check characters recorded). Such indicators provide a particularly useful readout for use in the periodic checking of the digital interface using suitable standard inputs (Sec. 4.3.8).

Once again storage of the selected word and the parity check characters is essential to enable these to be displayed. Such data will be referred to as “selected” data. Fig. 28 is a logic diagram of the selected data store. Control signal $I_n$ [Figs. 20, 21, 22 and 23] is inverted by buffer Q518A and enables the input data ($p_1$, $p_2$ and $b_0$ to $b_{15}$) to be read into the store, made up of 4-bit bistable latches, at appropriate times.

4.3.6. Displays

The display of data stored, as indicated in Sec. 4.3.5, is performed using the arrangement indicated in Fig. 29. A total of 20 numeric indicators is used; 8 for fixed data, 6 for time-of-day and 6 for the sampled data. For the fixed and the time-of-day data, decimal displays are used since such data are recorded in BCD. For the sampled data however an octal display is used which is generally the most convenient method of displaying the type of data recorded using the airborne data logger. Prior to the digital recording of data, analogue signals (representing the majority of the input data signals to be measured and recorded using digital techniques) are converted (using an airborne analogue to digital converter) to a 12 bit two’s complement digital word. A multiplier (or range indicator) in pure binary code is also generated and recorded. This gives the selected data display of the form indicated in Fig. 29.
To provide the numeric displays, appropriate outputs from the data stores (Figs. 27 and 28) are coupled to BCD to decimal decoders Q601 to Q620 which are in turn coupled to the numeric indicators V601 to V620. For the octal displays, inputs are applied only on the A, B and C lines to the BCD to decimal decoders and the D line is held permanently low. Interconnections between the store outputs and the display inputs (i.e. to the BCD to decimal decoders) have been tabulated in Appendix 2.

Parity error indication (in relation to the selected word only) is provided by lamps G1 and G2 driven via buffers Q621A and Q621B from the appropriate store outputs. Interconnections to the store are also indicated in Appendix 2.

4.3.7. Preset Stop Signal Generator for Analogue Tape Machine

The time-of-day information recorded on the magnetic tape effectively constitutes an identifier which may be used for specifying the location of any areas of interest on the tape. To enable the analogue tape machine to be stopped at any predetermined location, a preset stop signal generator [Fig. 30] has been incorporated in the digital interface.

Presetting of the required stop point of the tape transport is achieved using a total of 8 front panel mounted thumbwheel switches which allow time-of-day and day-of-the-month to be set. When the time-of-day and day-of-the-month read from the recorded tape corresponds with the information set on the thumbwheel switches a gating signal is generated which is transmitted to the tape transport (capable of being controlled by electrical signals applied from a remote location).

The thumbwheel switches are decoding types (Fig. 30) requiring complementary inputs and 8 diodes per switch. Normally the switch outputs Z₁ to Z₈ are low but when coincidence between the number set on any given switch and the decimal equivalent of the applied input is reached the output will switch to the high state. When coincidence is reached on all switches the output of the 8-input NAND gate Q701 will switch to the low state.

Interconnections between the thumbwheel switches and the appropriate outputs of the store of Fig. 27 have been tabulated in Appendix 3.

Since the store outputs may not all be set at precisely the same time it is essential that an inhibit signal be applied so that the output of the 8-input NAND gate is not interrogated at times when the data in the store are being changed. Control signal U (for the serial system [Figs. 20 and 21]) or U₁ (for the parallel system [Figs. 22 and 23]) may be used for this purpose, if the inhibit function applies when these signals are low. NAND gates Q702B (connected as an inverter) and Q702A produce the desired effect. A preset pulse (low state) is coupled to flip flop Q703 only if Z₁Z₂Z₃Z₄Z₅Z₆Z₇Z₈ = 1 and U (or U₁) = 1. Once having been preset (Q output set to the high state) the flip flop will remain in that state thus providing an output T buffered via NAND gate Q702C (connected as an inverter) which switches to and is maintained at the low state when coincidence of the preset data and the recorded data is reached.

Since at the moment of switch-on the Q output of flip flop Q703 may be either high or low it is essential that the flip flop be cleared (Q output set low) before the tape machine is set in motion (or an attempt is made to do so since if the Q output is high the machine will be stopped). Depressing the start pushbutton S709 prior to starting the tape machine ensures that the Q output of flip flop Q703 is high and hence that Q is low as required.

Since the digital data may be read at any tape speed in the range 1½ ips to 60 ips the machine would normally be run at maximum speed until the region of interest is reached. For precise location of the region of interest the tape machine could then be switched to a low speed (provided that the machine had been initially stopped a little "early.").
4.3.8. Serial Digital Data Generator

Overall checking of the digital interface is difficult using signals generated and recorded by the airborne digital data acquisition equipment. Such signals (e.g. those generated in the analogue to digital converter) generally vary with time. Moreover, under ideal conditions, no parity errors are detected in the reproduced data. A more useful method for checking the digital interface utilizes standard digital signals (having specified word composition) in which parity errors may be introduced to allow checkout of the parity circuits.

To provide such a check facility, conforming to the requirements of data to be recorded serially, an appropriate data generator (shown in block form in Fig. 31) has been developed. The data generator is a self-contained unit (powered from supply mains) which may be connected to the analogue tape recording machine or directly to the digital interface. The former connection allows the magnetic tape recording and reproducing processes to be conveniently checked. When recording is performed using NRZ techniques or when the generator is coupled directly to the digital interface, the NRZ1 output (which we will define as the “data” output) and the NRZ2 output (lateral parity output) are used. The RZ output is used only when recording using RZ techniques is required (since as indicated in Sec. 4.2 and Fig. 4 two outputs, NRZ1 and NRZ2, equivalent to the data and parity outputs of the NRZ reproducing conditioner, are produced by the RZ reproducing conditioner). EOW and EOR gaps, as required for the serial system, are generated.

Generation of suitable test data for the parallel system of recording is considered to be simpler as gaps are not required. Since a parallel recording facility has not so far been incorporated, no data generator has as yet been developed.

In the serial data generator shown in detail in Fig. 32 a variable frequency (640 hertz to 20-48 kilohertz to cover the required recording range) square wave input is required. Zener diode CR01 and resistor R01 ensure that the maximum allowable input level to the inverter Q01A is not exceeded.

A bit counter (Q02 and Q03) divides the input clock frequency by 20 (word generation) and a word counter (Q06 and Q08) divides the bit counter output frequency by any number presettable up to 100 (record generation). Front panel mounted decimal thumbwheel switches S04 (units) and S05 (tens) allow the number of words in a record to be preset. If, as indicated in Fig. 32, the thumbwheels are set to a reading of 16, then after 17 input pulses have been counted (since decade counters Q06 and Q08 were last reset to the “9” state), a reset-to-9 pulse will be propagated to these counters. Hence the word counter effectively divides by a number one greater than that set on the thumbwheels. To ensure that both counters are properly reset, a reset pulse stretching arrangement comprising Q010C, Q010B, C01 and R02 is incorporated. Using these components a reset pulse having a duration of at least about 300 nanosecond is provided.

Using 3-input NAND gate Q04A and dual input NAND gates Q05A and Q05B the bit counter is decoded to provide an inhibit signal (at the output of Q05A) which is subsequently used to insert EOW gaps in the data. Although an EOW gap of 2 bit durations is required for the serial data, gating has been provided which enables EOW gaps of 3 and 4 bit durations to be also generated. Longer EOW gaps allow the detection of certain marginal operating conditions.

The period of each word can be divided up into 20 equal time intervals associated with each bit which we will designate B0 to B19. In a logic context the symbol B9 (for instance) means that B9 is a quantity which takes on a high or a logical “one” value during the time interval associated with B9 and takes on a low or logical “zero” value at all other times. Define
a, b, c, d and e (as indicated in Fig. 32) as the respective bit counter outputs (where "a" is the least significant and so on). In the following table the logical outputs corresponding to each count state have been tabulated.

<table>
<thead>
<tr>
<th>Count Number</th>
<th>Counter Output Designation</th>
<th>Logical Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>e</td>
<td>d</td>
</tr>
<tr>
<td>0</td>
<td>B0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>B1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>B2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>B3</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>B4</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>B5</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>B6</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>B7</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>B8</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>B9</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>B10</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>B11</td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>B12</td>
<td>1</td>
</tr>
<tr>
<td>13</td>
<td>B13</td>
<td>1</td>
</tr>
<tr>
<td>14</td>
<td>B14</td>
<td>1</td>
</tr>
<tr>
<td>15</td>
<td>B15</td>
<td>1</td>
</tr>
<tr>
<td>16</td>
<td>B16</td>
<td>1</td>
</tr>
<tr>
<td>17</td>
<td>B17</td>
<td>1</td>
</tr>
<tr>
<td>18</td>
<td>B18</td>
<td>1</td>
</tr>
<tr>
<td>19</td>
<td>B19</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>B0</td>
<td>0</td>
</tr>
</tbody>
</table>

Further define the inhibit output of Q Q05A by the symbol $I_1$ (which must not be confused with a different quantity defined earlier in association with the digital interface).

For an EOW gap of 2 bit durations corresponding to B18 and B19

$$I_1 = (B18 + B19)' = (de)'$$

where $I_1$ is a quantity which is normally low but which takes on a high value for the time interval associated with B18 and B19.

Similarly for a 3-bit EOW gap

$$I_1 = (B17 + B18 + B19)' = [(abc + d)e]'$$

and for a 4-bit EOW gap

$$I_1 = (B16 + B17 + B18 + B19)' = [(bc + d)e]'$$

These alternative inhibit functions may be selected by switch S02.

In order to generate an EOR gap having a duration equivalent to that of one word (plus an EOW gap) another inhibit signal which we will define as $I_2$ is required. Decoding of the zero count state which will be present for the duration of a word for all settings of the switches S04 and S05 except the 00 setting, enables this inhibit signal to be generated. Defining word counter states as $W0$ etc. (in a similar manner to the B0 to B19 states defined for the bit counter) we may write

$$I_2 = (W0)'$$
The above inhibit function is generated using NOR gate Q01D and inverter Q01F. Further define a composite inhibit function $I$ generated at the output of NAND gate Q05C such that

$$I = (l_1l_2)' = W_0 + de$$

for an EOW gap of 2 bit durations.

Hence $I$ is a quantity which is normally low but which switches high for the time associated with the EOW and EOR gaps.

Using NOR gate Q01IC in association with the bit counter input signal $C_4$ (output of Q01B) allows a clock signal $C_t$ (interrupted during the EOW and EOR gaps) to be generated.

$$C_t = (C_4 + I)' = C_s(WE_0 + de)$$

for an EOW gap of 2 bit durations.

The form of the interrupted clock signal is indicated in the oscilloscope traces of Figs. 33(a) and 33(b). By suitably gating this clock signal to flip flops Q019A and Q019B (arranged to change state each time a clock signal is applied) appropriate NRZ data may be readily generated. Different word compositions are selected with switch S01 which allows a logic level of 0, 1, a, b, c, d, or e to effectively gate $C_t$. For generality define the output of switch S01 as $y$.

Some additional gating capability is provided by parity switch S03 having outputs defined as $x_1$ and $x_2$. The logical values of $x_1$ and $x_2$ for the three switch positions are tabulated below.

<table>
<thead>
<tr>
<th>Parity Switch</th>
<th>$x_1$</th>
<th>$x_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (ade')</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>(ade')</td>
</tr>
</tbody>
</table>

Note that ade' = B9.

Defining $D_1$ and $D_2$ as the clock signals used with flip flops Q019A and Q019B respectively for NRZ data generation we may write

$$D_1 = [C_t x_1(x_1y)']' = [C_t x_4(x_1' + y')]'$$

and

$$D_2 = (C_t y)'$$

For normal parity (position 2 of parity switch)

$$x_1 = x_2 = 1$$

and

$$D_1 = (C_t y)'$$

For position 1 of parity switch

$$D_1 = [C_t (B9 + y')]'$$

Hence, in this case, a clock pulse will always be generated at B9 irrespective of the form of $y$.

For position 3 of parity switch

$$D_1 = [C_t (B9)']'$$

In this case, a clock pulse will never be generated at B9 irrespective of the form of $y$.

For any given data input $y$ a parity error (either two "zeros" or two "ones") will be produced in either position 1 or position 3 of the parity switch but never in both positions.

Clocking of the NRZ output flip flops Q019A and Q019B (which takes place at the time of transition of the associated clock input from the high to the low state) has been arranged to take place a half period later than that of the counters to avoid spurious clock pulses which may be produced if both were clocked essentially at the same time.
Defining (as in Sec. 4.3.4) $b_n$, $b_1$ etc. as the digital information (either a “one” or a “zero”) contained in each data bit, we can draw up the following table for the various word compositions which may be selected via switch S03.

<table>
<thead>
<tr>
<th>Word Composition Switch Position</th>
<th>Data Bits (NRZ1 Output)</th>
<th>Longitudinal Parity</th>
</tr>
</thead>
<tbody>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1$</td>
<td>Even</td>
</tr>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0$</td>
<td>Even</td>
</tr>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$1 0 1 0 1 0 1 0 1 0 1 0$</td>
<td>Odd</td>
</tr>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$1 1 0 0 1 1 0 0 1 1 1 1 0 1 1 0 0$</td>
<td>Even</td>
</tr>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 0 0 0$</td>
<td>Even</td>
</tr>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1$</td>
<td>Even</td>
</tr>
<tr>
<td>$b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10}$</td>
<td>$1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0$</td>
<td>Even</td>
</tr>
</tbody>
</table>

The even longitudinal parity condition is not satisfied for the word composition as for switch position 2. Hence such a word composition may be used for checking the operation of the longitudinal parity circuits with the aid of the parity lamp used in the display. Using the sampled data display the above data are displayed in octal according to the following arrangement (see also Fig. 29).

<table>
<thead>
<tr>
<th>Word Composition Switch Position</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnitude</td>
<td>Multiplier</td>
</tr>
<tr>
<td>$b_0 b_1 b_2$</td>
<td>$b_0 b_1 b_2$</td>
</tr>
<tr>
<td>$b_3 b_4 b_5$</td>
<td>$b_3 b_4 b_5$</td>
</tr>
<tr>
<td>$b_6 b_7 b_8$</td>
<td>$b_6 b_7 b_8$</td>
</tr>
<tr>
<td>$b_9 b_{10}$</td>
<td>$b_9 b_{10}$</td>
</tr>
</tbody>
</table>

$b_{14}$ and $b_{15}$ correspond to the dummy bit and the longitudinal parity bit respectively and are not displayed. Hence octal displays according to the following table are produced with the various word compositions indicated.

<table>
<thead>
<tr>
<th>Word Composition Switch Position</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnitude</td>
<td>Multiplier</td>
</tr>
<tr>
<td>0</td>
<td>7777</td>
</tr>
<tr>
<td>1</td>
<td>0000</td>
</tr>
<tr>
<td>2</td>
<td>5252</td>
</tr>
<tr>
<td>3</td>
<td>6317</td>
</tr>
<tr>
<td>4</td>
<td>7417</td>
</tr>
<tr>
<td>5</td>
<td>7763</td>
</tr>
<tr>
<td>6</td>
<td>7774</td>
</tr>
</tbody>
</table>
Complementary digital information is always generated on the parity output NRZ2 (except when a lateral parity error is introduced via switch S03). If an odd parity error is introduced at B9 the NRZ1 output will change (and hence also the data displayed by the digital interface) but the NRZ2 output will not be affected. If the roles of the NRZ1 and the NRZ2 outputs are interchanged a complementary table to that above will result and the display will not be affected by the introduction of a parity error at B9.

With the data generator of Fig. 32 all words (except W0 constituting the EOR gap) are identical. If required, the EOR gap may be eliminated by using the 00 setting of switches S04 and S05 (for selecting the number of words per record). For that setting only EOW gaps are inserted. For any other setting of the switches, say to the number n for generality, each record will consist of n data words plus one EOR gap.

An RZ output for use with the analogue magnetic tape recording machine has also been provided (Fig. 32). The duration of the pulses used to saturate the tape in either a positive or negative sense (depending on whether a “one” or a “zero” is to be recorded [Sec. 4.2]) is set to 5 microsecond (independent of tape speed) using delay monostable Q012. Quad input NAND gates Q017A and Q017B generate 5 microsecond pulses to the low state (outputs normally high) on their respective outputs at appropriate times. Each of the following inputs is applied to these NAND gates:

(i) EOW and EOR gap inhibit signal J’ (normally high).

(ii) Positive pulses of 5 microsecond duration starting in time synchronism with the negative going transitions (i.e. from high to low state) of the input clock C.

(iii) Complementary outputs of flip flop Q018 for each gate respectively as set by the NRZ data output clocks D1 and D2.

(iv) A signal derived from the parity switch which allows the recording of information (either a “one” or a “zero”) to be inhibited at B9 if desired for checking purposes.

The outputs of Q017A and Q017B become the inputs to a discrete component switching circuit comprising transistors Q013 to Q016 and associated components. A low impedance RZ output is provided at the emitter of Q013. Positive pulses of 5 microsecond duration are produced when “ones” are generated and negative pulses of 5 microsecond duration are produced when “zeros” are generated.

To record data on the analogue tape machine the appropriate outputs (either NRZ or RZ) are taken to suitable recording amplifiers (plug-ins for tape machine) which convert these signals into the required recording head currents.

In Fig. 33 oscilloscope traces of the following signals (for word composition switch in position 3) are shown:

(i) Interrupted clock C.

(ii) NRZ1 output (parity normal).

(iii) NRZ2 output.

(iv) NRZ1 output with lateral parity error (in this case two “zeros” occurs at B9).

(v) RZ output (normal).

(vi) RZ output with missing bit at B9.

For the above signals two sets of photographs have been taken, one showing the waveforms over about a one word period and the other showing the same waveforms over a number of words but including also an EOR gap. Since for NRZ data the direction of switching has no significance the inversion of either the NRZ1 or the NRZ2 outputs does not represent any change in information.

5. CONCLUSION

To fulfill the ground station requirements for interpretation of data recorded on an airborne magnetic tape machine using both analogue and digital techniques:

(a) An analogue tape machine will be used in the first stage of reduction of data recorded using either analogue or digital techniques.

(b) A digital computer will be used in the final stage of reduction of data recorded using digital techniques. In many instances analogue data will be converted to digital form at the ground station and reduced using a digital computer.

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A digital interface capable of reading data over the full range of tape speeds available for the analogue reproducing machine will convert the special format digitally recorded data into a form which is convenient for most digital computers. Some special features of the digital interface are:

(i) A novel "electronic flywheel" circuit which enables the specially recorded serial digital data containing gaps to be read without the need for component switching for data rates varying over a 32 to 1 ratio.

(ii) A system for generating a signal which may be used to stop the analogue reproducing machine at any preselected time.

(iii) A special data generator which provides a rapid and convenient means of checking the operation of the digital interface (including the parity circuits).

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5. K. F. Fraser et al.  
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APPENDICES

1. COMPONENT DESCRIPTION

For ease of referring to the various circuit components, an identification consisting of a letter to indicate the class of component and a number which identifies each individual component are used.

The following letter classifications are used:
(i) R represents a resistor.
(ii) C represents a capacitor.
(iii) Q represents a solid state device (which may be a transistor or an integrated circuit).
(iv) S represents a mechanical switch.

The following number classifications are used:
(i) One or two digit numbers representing components in the signal conditioners (Sec. 4.2) used in conjunction with the analogue reproducing machine.
(ii) A three digit number, the first corresponding to a circuit number (1 to 7) and the remaining two to the individual component as used in the digital interface (Sec. 4.3.1 to 4.3.7).
(iii) A number similar to that for (i) prefixed by a “0” indicating that the component belongs to the serial digital data generator (Sec. 4.3.8).

In all circuits resistance and capacitance values are indicated respectively in ohm and in picofarad. Abbreviations “K” and “M” are also used where $K = 10^3$ and $M = 10^6$.

Thus for example a capacitance marked $1K$ has a capacitance of 1000 picofarad.
### 2. INTERCONNECTIONS BETWEEN DISPLAYS AND STORE

<table>
<thead>
<tr>
<th>Display Input</th>
<th>Display Unit Connected to Following Store Output</th>
<th>Display Input</th>
<th>Display Input Connected to Following Store Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q601A</td>
<td>Q506-1Q</td>
<td>Q611B</td>
<td>Q514-2Q</td>
</tr>
<tr>
<td>Q601B</td>
<td>Q506-2Q</td>
<td>Q611C</td>
<td>Q514-3Q</td>
</tr>
<tr>
<td>Q601C</td>
<td>Q506-3Q</td>
<td>Q611D</td>
<td>Logical 0</td>
</tr>
<tr>
<td>Q601D</td>
<td>Q506-4Q</td>
<td>Q612A</td>
<td>Q514-4Q</td>
</tr>
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<td>Q602A</td>
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<td>Q612B</td>
<td>Q515-1Q</td>
</tr>
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<td>Q612C</td>
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<td>Q516-2Q</td>
</tr>
<tr>
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<td>Q508-3Q</td>
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<td>Logical 0</td>
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### 3. INTERCONNECTIONS BETWEEN PRESET STOP SIGNAL GENERATOR AND STORE

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<th>Preset Stop Signal Generator Input Connected to Following Store Output</th>
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<td>S708A</td>
<td>Q513-3Q</td>
</tr>
<tr>
<td>S704A</td>
<td>Q514-1Q</td>
<td>S708A</td>
<td>Q513-3Q</td>
</tr>
<tr>
<td>S704B</td>
<td>Q514-2Q</td>
<td>S708B</td>
<td>Q513-4Q</td>
</tr>
<tr>
<td>S704B</td>
<td>Q514-2Q</td>
<td>S708B</td>
<td>Q513-4Q</td>
</tr>
<tr>
<td>S704C</td>
<td>Q514-3Q</td>
<td>S708C</td>
<td>Logical 0</td>
</tr>
<tr>
<td>S704C</td>
<td>Q514-3Q</td>
<td>S708C</td>
<td>Logical 0</td>
</tr>
<tr>
<td>S704D</td>
<td>Logical 0</td>
<td>S708D</td>
<td>Logical 0</td>
</tr>
<tr>
<td>S704D</td>
<td>Logical 0</td>
<td>S708D</td>
<td>Logical 0</td>
</tr>
</tbody>
</table>
BLOCK SCHEMA OF DATA PROCESSING SYSTEM

1. Recorded tape
2. Computer control
3. Preset stop
4. 7-channel analogue reproducer
5. NRZ digital data
6. Analogue data
7. Analogue to digital converter
8. Analogue reduction equipment
9. Digital interface
10. Read commands
11. Parallel digital data
12. Process stored data later
13. Small digital computer
14. Bulk memory (magnetic tape unit)
15. Computer compatible tape
16. File away
17. Take to large digital computer for detailed analysis
18. Printer
19. Plotter

SOFTWARE
PAPER TAPE READER
PROGRAM
DATA READOUT

M.E. REPORT 130
FIG. 1
DIGITAL WORD
RECORDED

NRZ
RECORDED SIGNAL

SIGNAL AT INPUT
OF NRZ REPRODUCE
CONDITIONER

NRZ OUTPUT
OF NRZ REPRODUCE
CONDITIONER

RZ
RECORDED SIGNAL

SIGNAL AT INPUT
OF RZ REPRODUCE
CONDITIONER

POSITIVE SCHMITT
OUTPUT OF RZ
REPRODUCE CONDITIONER

NEGATIVE SCHMITT
OUTPUT OF RZ
REPRODUCE CONDITIONER

NRZ1 OUTPUT
OF RZ REPRODUCE
CONDITIONER

NRZ2 OUTPUT
OF RZ REPRODUCE
CONDITIONER

WAVEFORMS RELATING TO REPRODUCING CONDITIONERS
SCHEMA OF NRZ REPRODUCING CONDITIONER
FIG. 4

NRZ REPRODUCING CONDITIONER

- 12 V

VARIABLE GAIN AMPLIFIER

FULL WAVE RECTIFIER

TRIGGER CIRCUIT

OUTPUT FLIP FLOP AND BUFFER

NOTE

+5V SUPPLY FOR Q5 AND Q6 DERIVED FROM +12V LINE USING ZENER DIODE AND RESISTOR

+12 V

NRZ OUTPUT
BLOCK SCHEMA OF RZ REPRODUCING CONDITIONER
VARIABLE GAIN AMPLIFIER

POSITIVE LEVEL AND NEGATIVE LEVEL SCHMITT TRIGGER CIRCUITS

PULSE TO NRZ CONVERTER

NOTE: +5V SUPPLY FOR Q52 AND Q56 TO Q60 DERIVED FROM +12V USING REGULATOR

RZ REPRODUCING CONDITIONER
NRZM
DATA

INPUT CLOCK SIGNAL GENERATOR

ELECTRONIC FLYWHEEL

OUTPUT CLOCK

CONTROL SIGNAL GENERATOR

SERIAL TO PARALLEL CONVERTER

DATA STORE

PRESET STOP SIGNAL GENERATOR

DIGITAL DATA DISPLAY

ANALOGUE REPRODUCE MACHINE CONTROL

WORD READ SYNC.

FRAME SYNC.

PARALLEL OUTPUT

TO DIGITAL COMPUTER

BLOCK SCHEMA OF DIGITAL INTERFACE
INPUT CLOCK SIGNAL GENERATOR FOR SERIAL SYSTEM
INPUT CLOCK SIGNAL GENERATOR FOR PARALLEL SYSTEM
(a) SIMPLE GAP DETECTION SYSTEM

(b) WAVEFORMS RELEVANT TO SIMPLE GAP DETECTION SYSTEM
(a) SEMI-AUTOMATIC SYSTEM OF GAP DETECTION EMPLOYING MISSING CLOCK PULSE INSERTION

(b) WAVEFORMS RELEVANT TO SEMI-AUTOMATIC SYSTEM OF GAP DETECTION, EMPLOYING MISSING CLOCK PULSE INSERTION
(a) FULLY AUTOMATIC (FLYWHEEL) SYSTEM OF GAP DETECTION EMPLOYING MISSING CLOCK PULSE INSERTION

(b) WAVEFORMS RELEVANT TO FULLY AUTOMATIC SYSTEM OF GAP DETECTION EMPLOYING MISSING CLOCK PULSE INSERTION
BLOCK SCHEMA OF THE COMPLETE ELECTRONIC FLYWHEEL
(a) SIMPLE PEAK DETECTOR

(b) PEAK DETECTOR USED
(a) 640 Hz INPUT CLOCK
   UPPER TRACE
   INPUT CLOCK A
   (HORIZ. SCALE: 5 sec. BETWEEN PULSES EXCEPT FOR GAPS)

   LOWER TRACE
   RAMP OUTPUT
   VERT SCALE: 2 VOLT/DIVN.

(b) 1.28 KHz INPUT CLOCK
   UPPER TRACE
   INPUT CLOCK A

   LOWER TRACE
   RAMP OUTPUT
   VERT. SCALE: 2 VOLT/DIVN.

(c) 2.56 KHz INPUT CLOCK
   UPPER TRACE
   INPUT CLOCK A

   LOWER TRACE
   RAMP OUTPUT
   VERT SCALE: 1 VOLT/DIVN.

RAMP OUTPUT OSCILLOSCOPE TRACES
(d) 5-12 KHz INPUT CLOCK

UPPER TRACE
INPUT CLOCK A

LOWER TRACE
RAMP OUTPUT
VERT. SCALE 0.5 VOLT/DIVN.

(e) 10-24 KHz INPUT CLOCK

UPPER TRACE
INPUT CLOCK A

LOWER TRACE
RAMP OUTPUT
VERT. SCALE 0.2 VOLT/DIVN.

(f) 20-48 KHz INPUT CLOCK

UPPER TRACE
INPUT CLOCK A

LOWER TRACE
RAMP OUTPUT
VERT. SCALE 0.1 VOLT/DIVN.

RAMP OUTPUT OSCILLOSCOPE TRACES
(a) OSCILLOSCOPE TRACES OF WAVEFORMS RELEVANT TO THE PEAK CHARGING CIRCUIT AT AN INPUT CLOCK FREQUENCY OF 640 HERTZ

(b) OSCILLOSCOPE TRACES INDICATING RELATION BETWEEN INPUT, INSERTED AND OUTPUT CLOCKS.
(a) OSCILLOSCOPE TRACE OF DESKEWED CLOCK IN THE VICINITY OF THE EOW GAP

(b) OSCILLOSCOPE TRACE OF DESKEWED CLOCK IN THE VICINITY OF THE EOR GAP
FLYWHEEL INSERTED
CLOCK-SERIAL SYSTEM
OR
RECORDED SYNCHRONIZING
DATA-PARALLEL SYSTEM

RESET

FLYWHEEL
OUTPUT
CLOCK

BIT
(COUNTER
(OR BYTE)
)

WORD & FRAME
SYNCHRONIZING
SIGNALS
GENERATOR

RESET

CONTROL
SIGNALS

COUNTER
OUTPUTS

SERIAL TO PARALLEL
CONVERTER CONTROL
SIGNAL GENERATOR

CONTROL
SIGNALS

DISPLAY CONTROL
SIGNAL GENERATOR

COUNTER
OUTPUTS

COUNTER
OUTPUTS

WORD
COUNTER

BLOCK SCHEMA FOR CONTROL SIGNAL GENERATOR FOR SERIAL
OR PARALLEL SYSTEMS
ANY WORD EXCEPT $W_0$ ($B_0$ TO $B_{19}$ IS ONE WORD DURATION)

FLYWHEEL OUTPUT CLOCK

FLYWHEEL DESKEWED CLOCK

CONTROL SIGNAL FOR USE WITH SERIAL TO PARALLEL CONVERTER (ALSO BIT COUNTER RESET)

CONTROL SIGNAL FOR USE WITH PRESET STOP SIGNAL GENERATOR

CLOCK SIGNAL FOR USE WITH SERIAL TO PARALLEL CONVERTER

READ COMMAND SIGNAL FOR DIGITAL COMPUTER

READ COMMAND SIGNAL FOR SAMPLED DATA DISPLAY - OCCURS ONLY FOR $W_1$

CONTROL SIGNAL FOR USE WITH FIXED DATA AND TIME-OF-DAY DISPLAYS - OCCURS ONLY FOR $W_1$

CONTROL SIGNAL FOR USE WITH FIXED DATA AND TIME-OF-DAY DISPLAYS - OCCURS ONLY FOR $W_1$

SECOND LAST WORD | LAST WORD IN RECORD | $W_0$ | $W_1$

FLYWHEEL INHIBIT AND FRAME SYNC. FOR DIGITAL COMPUTER

CONTROL SIGNAL FOR SERIAL TO PARALLEL CONVERTER

TIME RELATIONSHIP OF VARIOUS CONTROL SIGNALS FOR SERIAL SYSTEM
TIME RELATIONSHIP OF VARIOUS CONTROL SIGNALS FOR PARALLEL SYSTEM
LONGITUDINAL PARITY CHECK CIRCUIT

Q401A
\( V_1 \)\( \frac{1}{2} \)SN7404N

+5V

CLOCK

Q401B

J

R401 390

L

Q402D

P+R+P2

Q403A
\( V_2 \)SN7476N

CR

Q404A
\( V_2 \)SN7476N

Q404B

DATA FLIP FLOP

Q405A
\( V_2 \)SN7451N

LATERAL PARITY CHECK CIRCUIT

4-BIT SHIFT REGISTER

SERIAL TO PARALLEL CONVERTER FOR SERIAL SYSTEM

SERIAL INPUT

b15

b14

b13

b12

b11

b10

b9

b8

b7

b6

b5

b4

b3

b2

b1

b0

RIGHT SHIFT CLOCK
(1) CLOCK H
(2) DATA INPUT A₁
(3) CLEAR INPUT (A₁H)'
(4) PARITY INPUT A₂
(5) CLEAR INPUT (A₂H)'

(a) INPUT WAVEFORMS OBTAINED WHEN READING DIGITAL INFORMATION 1100 (PART OF WORD) FOR BIT RATE OF 20.48 KHz

(b) INPUT WAVEFORMS OBTAINED WHEN READING REPEATED DIGITAL WORD 110011001111001100 FOR BIT RATE OF 20.48 KHz AND INCLUDING EOR GAP

OSCILLOSCOPE TRACES OF INPUTS TO TEMPORARY STORAGE FLIP FLOPS (Q404 A&B) USED IN SERIAL TO PARALLEL CONVERTER (FOR SERIAL SYSTEM)
Q519—Q522  4-BIT BISTABLE LATCHES TYPE SN 7475 N
* PUT $P_2 = 0$ FOR PARALLEL SYSTEM

SELECTED DATA STORE
FIXED DATA

DECIMAL DISPLAYS

TIME OF DAY

SAMPLED DATA

OCTAL DISPLAY

ARRANGEMENT OF NUMERIC INDICATORS AND PARITY LAMPS.

DISPLAYS
Preset Stop Signal Generator

Inputs from Store

S702 to S708 (Contraves Type M531L)

R702 to R708

Q701

S709

Q702C (To Analogue Tape Machine)

Q703

SN7400N

Q702A

SN7470N

Q702B

FF

PR

CR

Inputs from Store

S702 to S708

Contraves Type M531L

Preset Stop Signal Generator
BLOCK SCHEMA OF SERIAL DIGITAL DATA GENERATOR
(a) WAVEFORMS OBTAINED OVER THE DURATION OF ONE WORD APPROXIMATELY FOR WORD COMPOSITION SWITCH SET TO POSITION 3

(b) WAVEFORMS OBTAINED OVER THE DURATION OF ONE RECORD APPROXIMATELY (FOR A RECORD CONTAINING THREE WORDS AND ONE EOR GAP) FOR WORD COMPOSITION SWITCH SET TO POSITION 3

OSCILLOSCOPE TRACES OF SOME WAVEFORMS RELATING TO THE SERIAL DIGITAL DATA GENERATOR